RIES50 FUNCTION GENERATOR

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OPERATION AND MAINTENANCE MANUAL

FUNCTION GENERATOR MODELS F52/F53

Serial No. _____

INTERSTATE ELECTRONICS CORPORATION
A Subsidiary Of A-T-O Inc.
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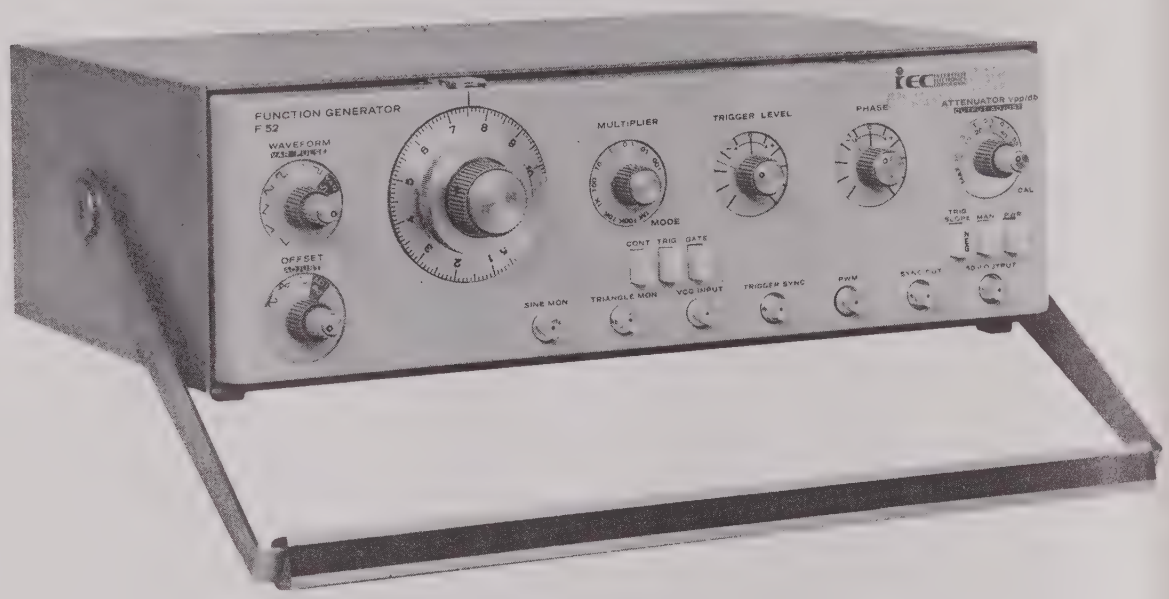

MODEL F52

MODEL F53

Figure 1-1. Function Generator MODEL F52/F53

Section I
GENERAL DESCRIPTION

1-1. INTRODUCTION

This manual has been carefully designed to complement the actual hardware design features of the Function Generator Models F52/F53 (figure 1-1) by providing detailed operation data, extensive maintenance, and performance test information. However, the function generators have been designed so that constant reference to the manual is not necessary in order to operate the equipment. The manual has been designed to provide the operator with an in-depth understanding of the functions, maintenance, and troubleshooting of the units, and to provide specific calibration laboratory tolerances, specifications, measurements, and adjustments in the event a malfunction occurs.

1-2. SPECIFICATIONS

Table 1-1 contains all key performance and physical specifications for the Function Generator Models F52/F53. Confirmation of performance within these specifications may be obtained by conducting the performance test routines presented in Section V of this manual. Outline mounting dimensions are shown in the installation diagram, figure 2-1.

1-3. DESCRIPTION

The Interstate Function Generator Models F52/F53 are state-of-the-art signal sources designed for great versatility, maximum ease of operation, and long operational life.

The case enclosing the function generators provides exceptional physical ruggedness and utility together with effective electrostatic shielding. The latter is important for the radio-frequency operating ranges of the instruments. Attention has been given to ground isolation applications and a grounding strap is provided at the rear of each instrument. The variable position handle permits the function generators to be tilted at the optimum angle for the operator. The handle facilitates carrying to new locations and serves as a cable strain relief when extended to the rear.

The serial number and other identification data are located on the metal plate at the rear of the instrument. This metal plate also serves as the primary heatsink for the power supply.

1-4. CAPABILITIES

The Function Generator Models F52/F53 selectably provides the following broad selection of output waveforms from the two 50 Ω OUTPUT front panel connection:

- Sine
- Square
- Triangle
- Ramp (15/85 duty cycle)

- Inverted ramp (85/15 duty cycle)
- Positive-going pulse (15 percent duty cycle)
- Negative-going pulse (15 percent duty cycle)
- Rectangular pulse with continuously variable duty cycle (100 nano-second minimum pulse width)
- Any of the above offset positively with respect to ground
- Any of the above offset negatively with respect to ground

In addition to these eight main output waveforms, there are three auxiliary fixed outputs continuously available at the front panel, each delivering 2 volts p-p in 50 ohms or 4 volts p-p (open). The three are:

- SINE MON (Auxiliary sine waveform)
- TRIANGLE MON (Auxiliary triangle waveform)
- SYNC OUT (Rectangular waveform)

There are three input BNC connectors which aid in the versatility of the F52/F53. These are:

- VCG INPUT (frequency modulates the output frequency)
- TRIGGER SYNC (triggers internal circuitry)
- PWM (pulse width modulates the variable output pulse)

The function generator also contains a phase-lock‡ control, in the one chassis. Almost any periodic signal can be phase locked from 10 Hz to 10 MHz.

A variety of trigger modes provide flexibility of the output waveform. Some of these trigger modes are:

- CONT (permits continuous operation of main generator)
- TRIG (permits internal or external triggering of main generator)
- GATE (inhibits or enables continuous operation)
- TRIG SLOPE/NEG (permits positive or negative triggering slope)
- MAN (manual trigger)

The calibrated frequency range of the function generator is from 0.0005 Hz to 10 MHz in 10 ranges each covering a 20:1 ratio. External signals may be applied at the front panel to frequency modulate the main signal output by as much as 100:1. The generator output frequency may be locked to an input reference by applying the external signal to the front-panel TRIGGER SYNC connector.

A total output level variation of greater than 70 db may be realized with the 50 db calibrated step attenuator in combination with the 20 db variable attenuator. Maximum output level is 30 volts peak-to-peak into an open circuit (15 volts p-p into 50 ohms).

Any waveform may be manually offset up to ±10 volts subject to the limitation that the total voltage swing (d-c plug signal peak) may not exceed ±15 volts into an open circuit.

‡The Model F52 does not provide the phase-lock feature.

TABLE 1-1. TECHNICAL SPECIFICATIONS

Parameter	Characteristics
Waveforms	
Variable Amplitude	Sinewave Squarewave Triangle wave 15/85% duty cycle positive pulse 15/85% duty cycle negative pulse 15/85% duty cycle positive ramp 15/85% duty cycle negative ramp Variable duty cycle pulses, 5 to 95% of full duty cycle (100 nsec minimum) All waveforms symmetrical with respect to ground Output impedance: 50 ohms
Simultaneous Fixed Amplitude Monitors	Sine, square (SYNC OUT), and triangle. Sine, square, and triangle assume 15/85% duty cycle when fixed duty cycle ramps or pulses are selected. All monitors are 2 volts p-p, 50-ohm impedance, balanced with respect to ground. SYNC OUT rise time: < 20 nsec. All monitor signals 180 degrees out of phase with main output. Squarewave (SYNC OUT) leads sine and triangle by 90 degrees.
Frequency	
Range	Sine, square, or triangle waveforms: 0.0005 Hz to 10 MHz. Ramps and pulse waveforms: 0.0005 Hz to 5 MHz. Triggered and gated waveform: 0.0005 Hz to 3 MHz. Ten decade ranges with 50% overlap provide 20:1 continuous vernier adjustment within any range.

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Table 1-1. Technical Specifications (Continued)

Parameter	Characteristics
Dial Accuracy	Sine, square, or triangle waveforms: < ±1% of setting ±1 minor division, 0.0005 Hz to 500 kHz. < ±3% of setting ±2 minor division, 500 kHz to 5 MHz. < ±5% of setting ±3 minor division, 5 MHz to 10 MHz. 15/85% duty cycle ramps and pulses: < ±1% of setting ±1 minor dial division 0.0005Hz to 500 kHz. < ±10% of setting ±1 minor dial division 500 kHz to 5 MHz.
Stability	< ±0.05% of setting for 10 minutes. < ±0.25% of setting for 24 hours.
Time Symmetry	< 1%, 0.0005 Hz to 10 Hz <0.5%, 10 Hz to 100 kHz < 2%, 100 kHz to 3 MHz
Amplitude	
Attenuator	Precision 2% attenuator calibrated in db and volts peak-to-peak in 10-db steps from 0 db to -50 db (0 db = 10 volts p-p into 50-ohm load). Uncalibrated MAX position provides approximately +3 db maximum output (15 volts p-p). Continuously variable control provides additional 0-db to 20-db attenuation at any step. Minimum output is 70 db below 10 volts p-p (3 mv p-p).

Table 1-1. Technical Specifications (Continued)

Parameter	Characteristics
Amplitude Response	Sinewave (Ref: 10 volts p-p (3.5 vrms) into 50-ohms at 1 kHz): <±0.5%, 0.0005 Hz to 100 kHz <±1%, 100 kHz to 1 MHz <±3%, 1 MHz to 5 MHz <±10%, 5 MHz to 10 MHz Triangle or square waveforms (Ref: 10 volts p-p into 50 ohms at 1 kHz): <±3%, 0.0005 Hz to 1 MHz <±10%, 1 MHz to 10 MHz
Maximum Usable Output* (50-Ohm Load)	Sine, square, or triangle waveforms: >15 volts p-p, 0.0005 Hz to 5 MHz >10 volts p-p, 5 MHz to 10 MHz Ramps and Pulses: >15 volts p-p, 0.0005 Hz to 3 MHz >12 volts p-p, 3 MHz to 5 MHz *With open circuit, maximum output level is twice that specified with 50-ohm load.
Amplitude Differential	P-P differential between sine, triangle, or square waveforms: 5%, 0.0005 Hz to 5 MHz
Rise Times	Squarewave or 15/85% pulses: 30 nsec Variable duty cycle pulses: 50 nsec
Sinewave Distortion (Ref: 10 Vpp into 50 ohms)	<0.5%, 0.0005 Hz to 100 kHz <1.0%, 100 kHz to 1 MHz <3.0%, 1 MHz to 5 MHz <5.0%, 5 MHz to 10 MHz
Triangle Nonlinearity (Ref: 10 Vpp into 50 ohms)	<1%, 0.0005 Hz to 100 kHz <5%, 100 kHz to 5 MHz

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Table 1-1. Technical Specifications (Continued)

Parameter	Characteristics
Rectangular Wave Aberrations	<5%, 0.0005 Hz to 5 MHz
Amplitude Stability	<±0.05% of specified maximum p-p output for 10 minutes. <±0.25% of specified maximum p-p output for 24 hours.
Offset Stability	<±0.25% of maximum specified p-p amplitude over any 72-hour period.
Modulation	
Output Frequency (VCG)	Controlled with an external voltage applied at the VCG INPUT. Linear to within 0.2% on all ranges except 1 M. An input of 0 to +10 volts increases frequency as much as 100:1 from minimum dial setting. An input of 0 to -10 volts decreases frequency as much as 100:1 from maximum dial setting. VCG bandwidth: 100 kHz Input impedance: 10k ohms
Variable Duty-Cycle Pulse Width	Controllable with an external voltage applied at the PWM input (linear to within 1%). With the front panel control (VAR ⎍) centered, 0 to ±10 volts varies duty cycle 5 to 95% (100 nsec minimum). PWM bandwidth: 10 kHz Input impedance: 2k ohms

Table 1-1. Technical Specifications (Continued)

Parameter	Characteristics
External Sync Input	Periodic waveforms >5 volts p-p (100-volt maximum) at TRIGGER SYNC input synchronizes the output frequency when within 0 to -1% of the external frequency. (Pulse input waveforms are required at 100k and 1M ranges.) Input impedance: 10k ohms
Phase-Lock‡	Main generator output will automatically phase-lock to the fundamental of any periodic external signal >±1 volt (100-volt maximum) applied to the TRIGGER SYNC input. (Zero Phase Setting) Phase between input and output adjustable to ±180 degrees with PHASE control. (Decreasing above 200 kHz) Generator output may be locked to any harmonic or subharmonic through the fifth order of the external frequency by adjusting phase control and observing on scope. Input/Output frequency range: 10 Hz to 10 MHz (with frequency dial set to output frequency between 1.0 and 10). Input impedance: 10k ohms ϕ LOCK indicator lights only when phase-locked to fundamental input frequency. Blinking light indicates no trigger.‡
DC Offset	Selectable (1) 0 volts dc

‡The Model F52 does not provide the phase-lock feature.

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Table 1-1. Technical Specifications (Continued)

Parameter	Characteristics
	(2) Positive fixed } Peaks tangent to 0 volts dc, output reduced to one-half amplitude (3) Negative fixed } (4) Variable: Adjustable between ±10 volts into an open circuit (signal plus offset is <±15 volts). Variable offset independent of variable attenuator setting only in MAX and 0 db attenuator position.
Trigger	Manual or external signal >±1 volt (100-volt maximum) at TRIGGER SYNC input initiates one complete trigger cycle. Cycle start/stop point continuously variable ±90 degrees with PHASE control. TRIGGER LEVEL control and TRIG SLOPE pushbutton determine any triggering point on input waveform. Input Impedance: 10k ohms.
Gate	Manual or external signal >±1 volt (100-volt maximum) at TRIGGER SYNC input gates main generator output on for the duration of the gate signal. Last cycle is completed after gate is removed.
Isolation	Detachable ground strap may be removed to isolate all BNC connectors and circuit grounds from case and power line ground. Maximum isolation: ±500 volts

Table 1-1. Technical Specifications (Continued)

Parameter	Characteristics
Operating Temperature	0 to 55°C
Power	115 vac ±10% or 230 vac ±10%, 50 to 400 Hz, 50 watts maximum.

NOTES:

Except where indicated, specifications apply with 25° ±10°C ambient, with 50-ohm resistive load, 0-vdc offset, frequency control set between 1.0 and 10.0 on the frequency dial. All external inputs removed.

Section II
INSTALLATION

2-1. INTRODUCTION

This section provides instructions pertaining to receiving, inspecting, and installing the equipment.

2-2. RECEIVING AND INSPECTION

Immediately upon receipt of the instrument, the exterior of the shipping container should be insepcted for physical damage and the carrier notified if such is visible. After carefully removing all packing materials, the instrument should be inspected to ensure that it is free of all mars and blemishes.

Electrical performance that meets or exceeds the specifications (Section I, table 1-1) should be confirmed as soon as possible. Section V contains a suggested performance test routine and lists the recommended test equipment.

2-3. INSTALLATION

This instrument may be used on the workbench or rigidly mounted in a RETMA rack structure by means of an optional rack-mounting kit (see figure 2-1 for details of single and double unit rack assemblies). As initially shipped, the instrument is provided with a rugged, adjustable handle that facilitates carrying as well as tilting for optimum panel viewing angle.

This all solid-state instrument requires no special cooling facilities as long as it is operated within the temperature limits specified in table 1-1.

2-4. POWER REQUIREMENTS

This instrument operates from a-c power only, either 115 or 230 vac, 50 to 400 Hz. A slide switch at the rear of the equipment readily selects the desired power line voltage.

CAUTION

Operation at the wrong power line voltage switch setting may damage the instrument.

A three-conductor cord is supplied with the equipment to permit referencing the chassis and case to power system ground. This safety feature is recommended by the National Electrical Manufacturers Association (NEMA). The offset pin on the power cord connector is the ground wire.

2-5. REPACKAGING

If it becomes necessary to pack the instrument for shipment, the following procedure is recommended.

a. Attach a tag with the owner's name, address, and telephone number together with a brief description of the purpose of the shipment and the date its return is desired.

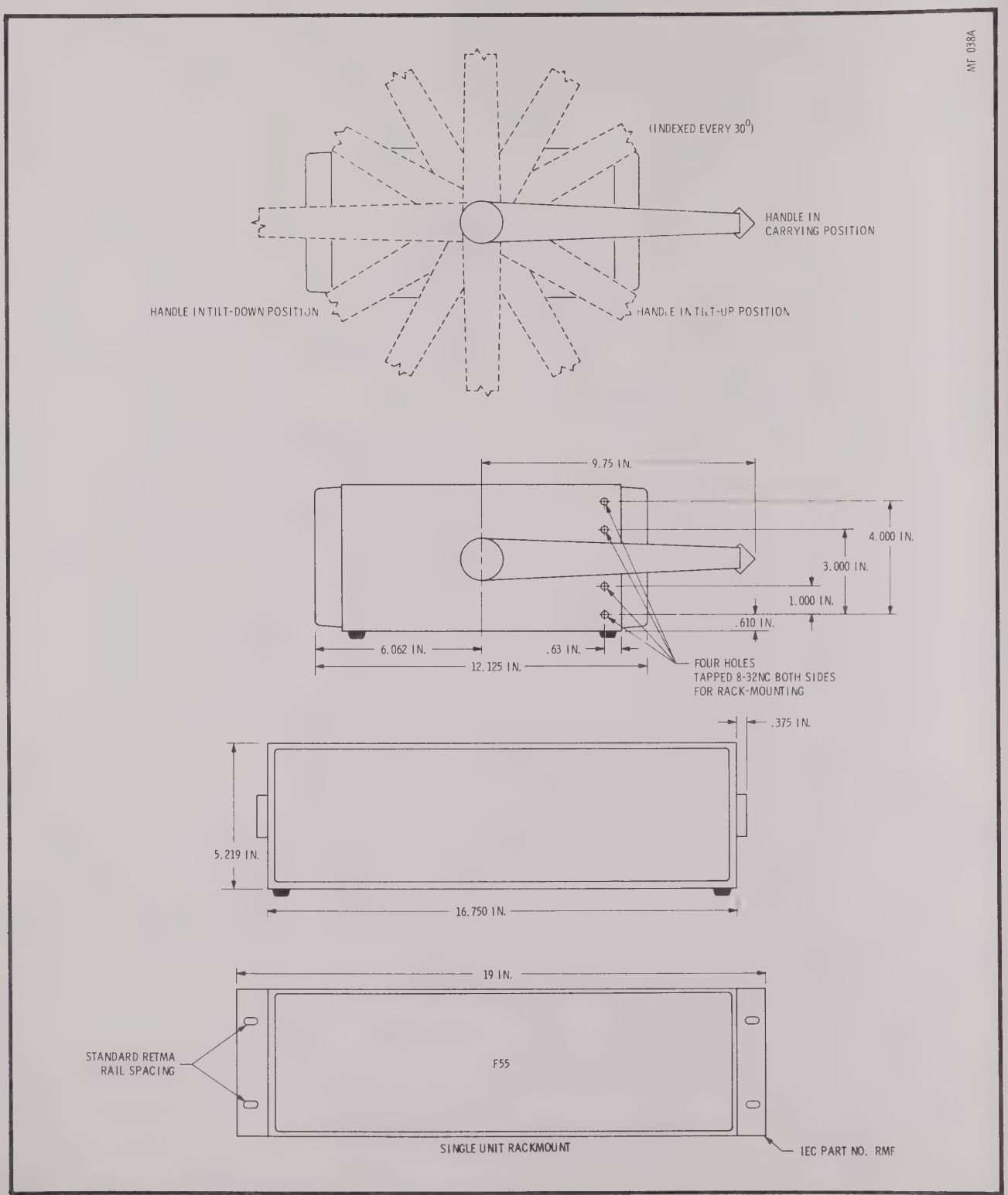


Figure 2-1. Installation Detail

b. Wrap the equipment in heavy paper or plastic before placing in an inner container.

c. Use soft packing material liberally around all sides of the instrument inside the inner container.

d. Enclose the inner container in a rugged carton or wood box with suitable packaging material to prevent movement in any direction and seal the outer container with heavy tape or metal bands.

e. Mark the shipping container with the shipping address and "DELICATE INSTRUMENT" labels.

2-6. DISASSEMBLY

To remove the function generator from its case, remove the three retaining screws mounted in the heatsinks at the rear of the unit and one screw from the ground strap and withdraw the chassis through the front of the case.

(1) Remove the four screws (two upper, and two lower) from the top and bottom of the front faceplate (figure 2-2). This will expose the upper and lower front subpanels and controls.

(2) Remove the two retaining screws at the bottom of the A2 board, near the front, outer edges. These screws are seated in two spacers permanently mounted on the A1 board. The A1 and A2 boards, and their respective front subpanels, will then open book-fashion at the front edges.

NOTE

The screw-hinge assembly at the rear of the A2 board is a permanent fixture and need not be dismantled or removed to gain normal access to the boards.

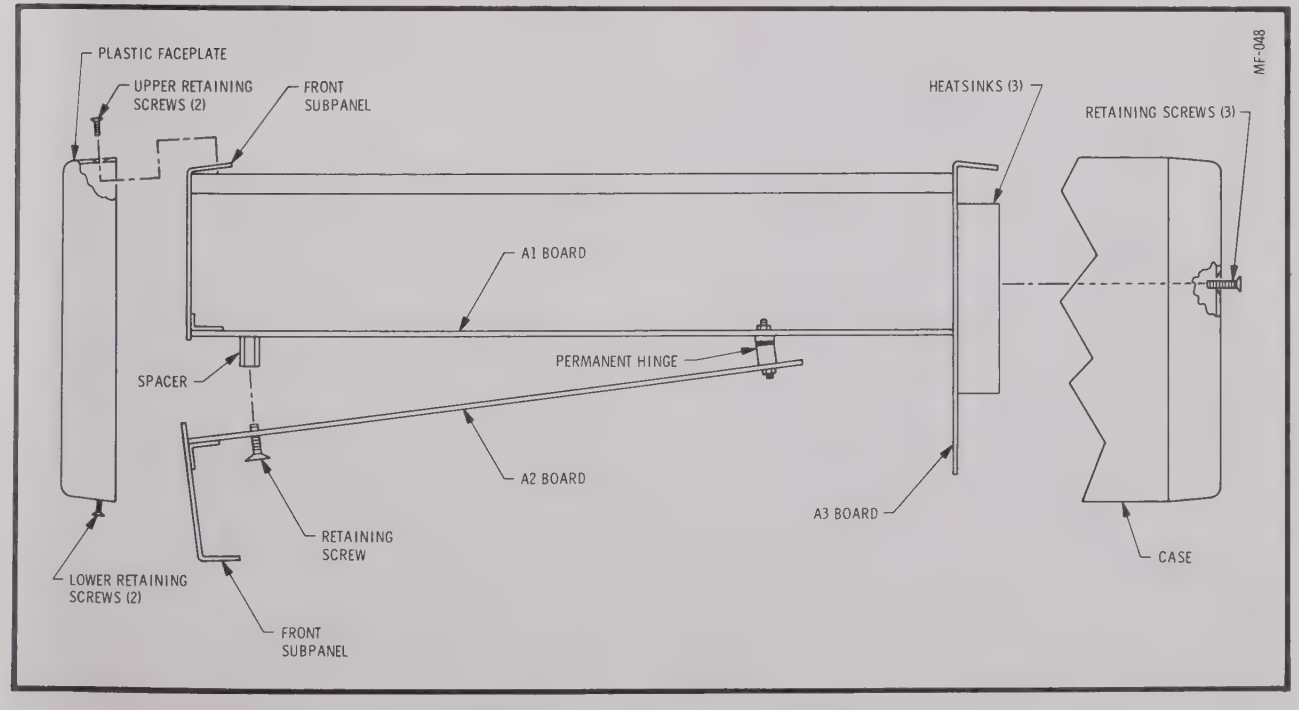


Figure 2-2. Disassembly Diagram

Section III
OPERATING INSTRUCTIONS

3-1. INTRODUCTION

Operation of the function generator is relatively simple and straightforward. Normally, an operator can expect to realize the full potential of the instrument without reference to the manual; however, this section provides operating tips and will assist those unfamiliar with this type of equipment. Refer to figures 3-1 and 3-2 for identification of front and rear panel controls and indicators.

3-2. GENERAL INFORMATION

Power is applied to the function generator by pressing the PWR pushbutton. A neon pilot indicator located at the frequency dial cursor indicates that power is applied to the unit.

Pressing the CONT MODE pushbutton will permit normal output operation of the function generator.

The calibrated 20:1 frequency dial provides a 50 percent overlap with adjacent bands as selected by the MULTIPLIER range switch. The ten decades of the MULTIPLIER switch permit the instrument to be tuned over the frequency range of 0.0005 Hz to 10 MHz.

Any of the eight standard waveforms may be selected with the WAVEFORM switch. The concentric VAR PULSE control (inhibited except when the variable pulse is selected by the WAVEFORM switch) permits varying the duty cycle of a rectangular waveform.

The desired output waveform is provided at the 50 Ω OUTPUT connector.

The OFFSET switch establishes the waveform polarity with respect to ground. The output may be selected to be symmetrically all positive, all negative, or continuously adjustable about ground. The concentric ADJUST offset control (inhibited except in the ADJ position of the OFFSET switch) provides ±10 volts offset into an open circuit and ±5 volts into a 50-ohm load.

The frequency of the instrument may be varied by an external voltage applied to the VCG INPUT connector on the front panel. A full 100:1 frequency change may be obtained from +10 volts when the frequency dial is set at the low limit, and conversely, from -10 volts with the frequency dial set at the upper limit.

The SYNC OUTPUT signal is a 4 volt p-p open circuit (2 volts p-p into 50 ohms) rectangular wave that, on its positive transition, leads all symmetrical waveforms at main output by 90 degrees. The SYNC OUT signal assumes the same duty cycle as the fixed ramp and pulse outputs; however, for variable pulse width operation, SYNC OUT is 50/50 duty cycle.

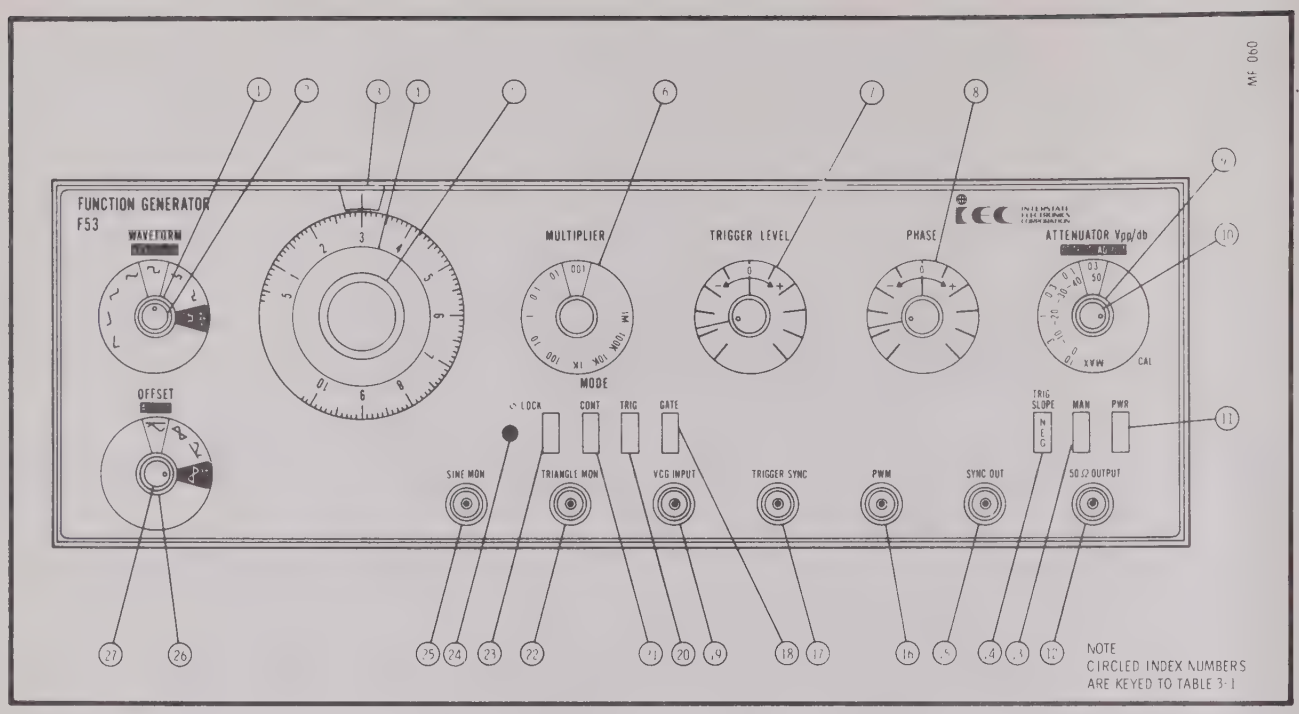


Figure 3-1. Controls and Indicators

TABLE 3-1. FUNCTIONS OF CONTROLS AND INDICATORS

Index No.	Function
1	WAVEFORM switch: Selects desired output waveform; activates VAR PULSE control.
2	VAR PULSE control: Potentiometer varies duty cycle of output pulse when WAVEFORM switch is set to VAR ⎍ position.
3	Dial Cursor/Pilot indicator: Glows when power is applied to the unit.
4	Frequency dial, coarse control: Adjusts frequency dial in 1:1 rotation ratio.
5	Frequency dial, fine control: Adjusts frequency dial in 6:1 rotation ratio.
6	MULTIPLIER switch: Rotary switch selects multiplying factor for frequency setting.
7	TRIGGER LEVEL control: Potentiometer selects triggering point on incoming signal to trigger output waveform.
8	PHASE control: Potentiometer adjusts phase ±180^{O} with output waveform when in ϕ LOCK MODE; adjusts point (phase) of starting and stopping output waveform when in TRIG MODE.
9	ATTENUATOR switch: Rotary switch attenuates the output signal in five steps of 10 db per step. Calibrated in Vpp and db.

Table 3-1. Functions of Controls and Indicators (Continued)

Index No.	Function
10	OUTPUT ADJUST control: Potentiometer provides additional 20 db attenuation of the output amplitude.
11	PWR pushbutton: Power on/off control; when power is applied, dial cursor will illuminate.
12	50 Ω OUTPUT terminal: Output BNC connector for all waveforms. Maximum output level is 30 volts p-p (open) or 15 volts p-p (into 50 ohms).
13	MAN pushbutton: Provides manual input trigger.
14	TRIG SLOPE (NEG) pushbutton: Selects triggering slope of incoming signal; pressed to select negative slope only.
15	SYNC OUT terminal: Output BNC connector provides rectangular waveform 180^{O} out of phase with the 50 Ω OUTPUT squarewave signal (2 volts p-p into 50 ohms).
16	PWM terminal: Input BNC connector for modulating the output pulse width when VAR ⎍ waveform is selected.
17	TRIGGER SYNC terminal: Input BNC connector synchronizes output waveform with input in CONT or ϕ LOCK‡ MODES. Provides trigger input signal to trigger the output waveform when in TRIG or GATE MODE.
18	GATE MODE pushbutton· Allows TRIGGER SYNC input signal to enable the main output waveform.
19	VCG INPUT terminal: BNC connector provides for external voltage control of the output frequency.
20	TRIG MODE pushbutton: Allows TRIGGER SYNC input signal or MAN pushbutton to trigger one cycle of the main output waveform.
21	CONT MODE pushbutton: Provides for selection of continuous operation of the main output waveform.
22	TRIANGLE MON terminal: BNC connector provides auxiliary triangle output waveform (2 volts p-p into 50 ohms).
23	ϕ LOCK pushbutton‡: Allows output waveform frequency to track input TRIGGER SYNC frequency.
24	ϕ LOCK indicator‡: Glows when output frequency is locked to fundamental frequency of TRIGGER SYNC.
25	SINE MON terminal: BCN connector for auxiliary sinewave output (2 volts p-p into 50 ohms).

‡The Model F52 does not provide the phase-lock feature.

Table 3-1. Functions of Controls and Indicators (Continued)

Index No.	Function
26	OFFSET switch: Rotary switch selects waveform, offset with respect to ground. Positive and negative going functions are half amplitude as compared to functions symmetrical about ground.
27	ADJUST (OFFSET) control: Potentiometer provides continuously variable d-c offset when the OFFSET switch is in the ADJ ⏦ position.

3-3. OPERATING INFORMATION

The PHASE control performs a dual function: (1) when in the LOCK MODE, the PHASE control varies the output phase ±180 degrees relative to the input phase, and (2) when in TRIG or GATE MODE the PHASE control determines the starting point (phase of the first cycle and the stopping point of the last cycle.

The TRIGGER LEVEL control determines the exact point on the TRIGGER SYNC input signal needed to trigger the internal logic.

The TRIG SLOPE (NEG) pushbutton, when pressed, will select the negative edge of the TRIGGER SYNC input signal; otherwise, it selects the positive edge.

Pressing the CONT MODE pushbutton provides continuous operation of the main function generator frequency and allows all waveforms to be available at the 50 OUTPUT terminal.

Pressing the TRIG MODE pushbutton disables the main frequency until a TRIGGER SYNC input signal is received or until the MAN (manual trigger) pushbutton is pressed. Only one cycle of the main output frequency is produced per one trigger cycle.

Pressing the GATE MODE pushbutton also disables the main frequency until a TRIGGER SYNC input signal is received or until the MAN (manual trigger) pushbutton is pressed; however, in GATE MODE, the output frequency operation continues for the duration of the gate signal.

Pressing the ϕ LOCK MODE‡ pushbutton allows the output frequency to track any periodic TRIGGER SYNC input signal. The output frequency can be phase-locked to any periodic input signal from 10 Hz to 10 MHz when within the proper frequency range controls on the front panel. The phase-lock circuitry is capable of locking onto harmonics (up to the fifth) and subharmonics (down to the fifth) while observing the input and output on an oscilloscope. However, the ϕ LOCK indicator will only illuminate when the output generation frequency is identical to the TRIGGER SYNC input frequency.‡

The ATTENUATOR Vpp/db switch is a 50 db (calibrated 10 db per step) attenuator from 10 volts p-p to 0.03 volts p-p, with a 30 db continuously variable OUTPUT ADJUST control. The MAX position on the face of the ATTENUATOR switch is not calibrated but provides 30 volts p-p (open) or 15 volts p-p (into 50 ohms). A total of 70 db attenuation can be

‡The Model F52 does not provide the phase-lock feature.

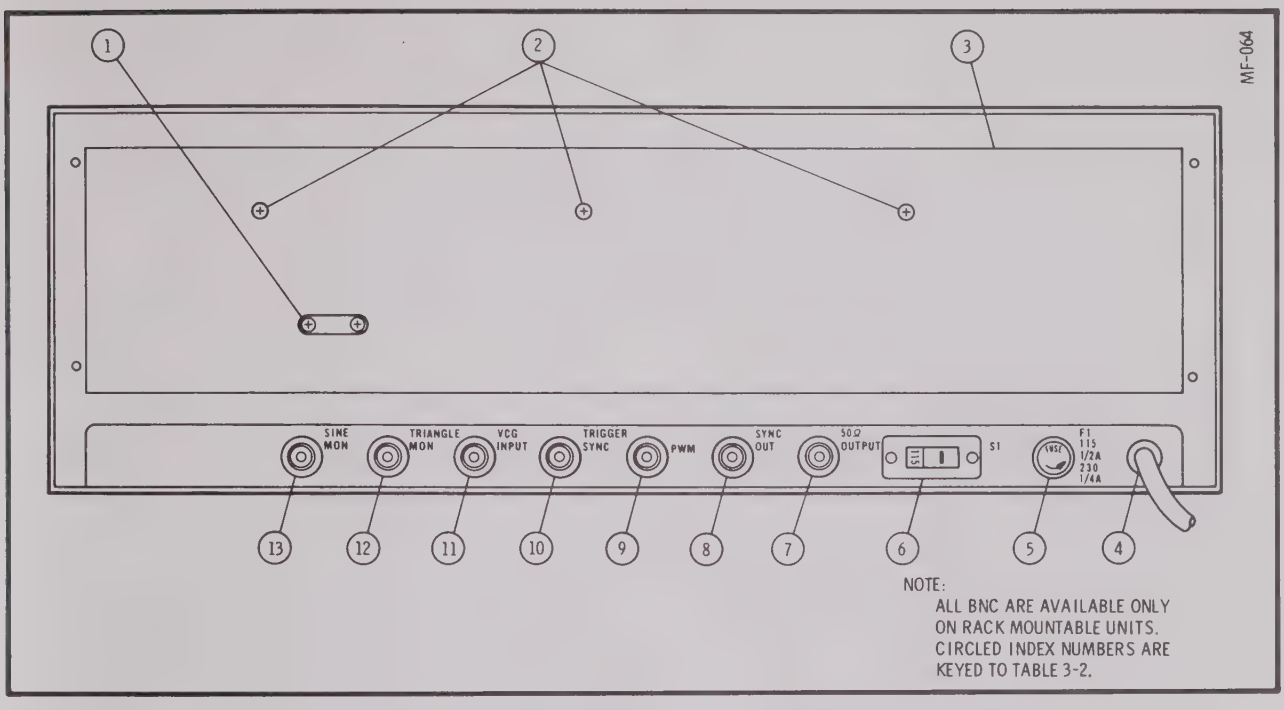


Figure 3-2. Real Panel Connectors and Fuse

TABLE 3-2. FUNCTIONS OF REAR PANEL CONNECTORS AND FUSE

Index No.	Function
1	Ground Strap: Permits signal ground to be isolated from case ground.
2	Retaining Screws: Mounted in heatsinks: remove to dismantle the unit.
3	Rear Panel: Primary Heatsink for power supply.
4	Line Cord: Three-wire type cord permits grounding of case.
5	Fuse: Slo-Blo, 1/2 Amp. 115 VAC; 1/4 Amp. 230 VAC.
6	Line Voltage Switch: Selects 115 VAC or 230 VAC.
7	50 Ω OUTPUT terminal: Output BNC connector for all waveforms. Maximum output level is 30 volts p-p (open) or 15 volts p-p (into 50 ohms).
8	SYNC OUT terminal: Output BNC connector provides rectangular waveform 180° out of phase with the 50Ω OUTPUT squarewave signal (2 volts p-p into 50 ohms).
9	PWM terminal: Input BNC connector for modulating the output pulse when VAR ⎍ waveform is selected.

Table 3-2. Functions of Rear Panel Connectors and Fuse (Continued)

Index No.	Function
10	TRIGGER SYNC terminal: Input BNC connector synchronizes output waveform with input signal when in CONT MODE. Provides trigger input signal to trigger the output waveform when in TRIG or GATE MODE.
11	VCG INPUT terminal: BNC connector provides for external voltage control of the output frequency.
12	TRIANGLE MON terminal: BNC connector provides auxiliary triangle output waveform (2 volts p-p into 50 ohms).
13	SINE MON terminal: BNC connector for auxiliary sinewave output (2 volts p-p into 50 ohms).

achieved by the combined function of both attenuator controls.

CAUTION

Disconnect any external input to the TRIGGER SYNC terminal when not in use so that waveforms are not perturbed by accidental TRIGGER SYNC input signals.

3-4 OPERATING TIPS

a. FREQUENCY MODULATION. - Any output frequency may be frequency modulated up to a 100 kHz rate with an a-c signal of peak-to-peak value less than 10 volts.

b. OFFSET. - The sum of the d-c offset plus the signal peak value can not exceed ±15 volts into an open circuit (±7.5 volts into 50 ohms).

c. PULSES AND RAMPS. - The extremely fast rise times and slew rates of the function generator circuitry permit practical pulse durations of less than 100 nanoseconds. However, pulse and ramp waveforms above 5 MHz (200 nsec period) will experience degradation with increasing frequency. The fastest possible rise times (less than 20 nanoseconds) are available at the SYNC OUT terminal because of the reduced, fixed amplitude. It will be noted that the nature of the variable pulse-width circuits causes a variable delay between the SYNC OUT and the 50 Ω OUTPUT waveform as the pulse width is adjusted.

d. WAVEFORM PURITY. - The 50 percent frequency overlap of adjacent ranges will often make it possible to tune to the desired frequency on either of two MULTIPLIER ranges. Select the lower MULTIPLIER range for maximum waveform purity.

e. PWM INPUT. - PWM input remotely controls the pulse width of the output pulse when the WAVEFORM switch is set in the VAR ⎍ position.

f. TRIGGER SLOPE. - The TRIG SLOPE (NEG) pushbutton is pressed only when the negative triggering edge is desired; otherwise the positive edge is used for the trigger input.

Section IV
THEORY OF OPERATION

4-1. INTRODUCTION

This section contains a detailed functional description of the function generator. Each functional section is discussed with its own block diagram to facilitate easy understanding.

4-2. OVERALL FUCTIONAL DESCRIPTION

The complete block diagram is shown in figure 4-1. This diagram illustrates the interrelationships of all of the functional sections which are discussed in the following paragraphs. A more detailed block diagram is shown in figure 7-1, and circuit board detailed schematics are shown in figures 7-3, 7-5, and 7-7.

The function generator can be divided into 12 functional sections. Each of these is explained in a logical progression:

- Frequency Control
- Voltage-to-Current Converter
- Triangle Amplifier
- Inverter Amplifier
- Automatic Level Control
- Voltage Level Sensor
- Sine Shaper
- Variable Pulse Width Shaper
- Output Amplifiers
- Trigger Logic
- Phase Lock Control‡
- Power Supply

4-3. FREQUENCY CONTROL AND VOLTAGE-TO-CURRENT CONVERTER

The frequency control section makes up the "front end" of the function generator. Inputs are single-ended control voltages from the main frequency potentiometer or from an external voltage source. The voltages are scaled, inverted, and offset by the frequency control circuits.

The voltage-to-current converter interfaces with four related output voltages from the frequency control section. By means of precision resistor networks and closed-loop amplifiers, these voltages are converted to proportional, equal and opposite, switchable currents. The currents, of appropriate magnitude, when switched into an integrating capacitor, under controlled conditions, determine the frequency of the function generator.

Figures 4-2 and 4-3 show the essential elements of the frequency control and voltage-to-current converter circuits in block diagram form.

a. FREQUENCY CONTROL. - As shown in figure 4-2, two controlling voltages (from the main frequency dial control or from an external source, if used) are summed at the input to the first inverting amplifier. A fixed, positive

‡The Model F52 does not provide the phase-lock feature.

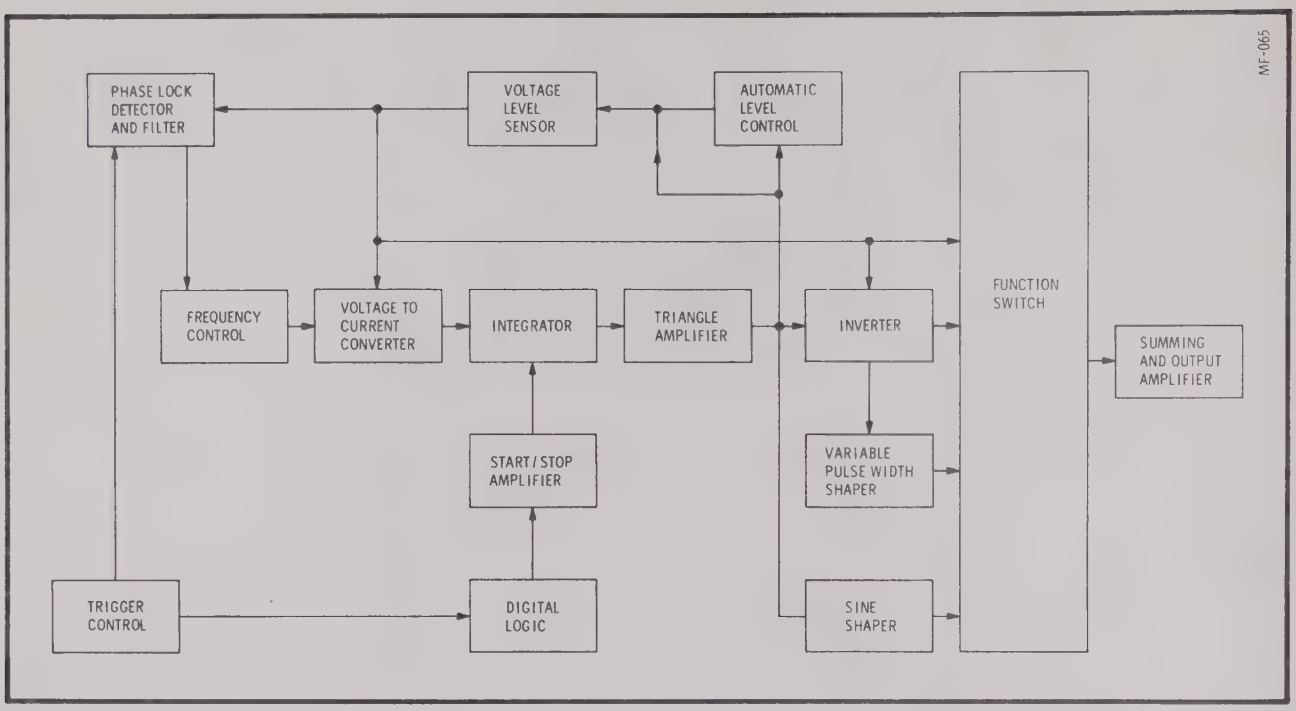


Figure 4-1. Simplified Block Diagram

level offset voltage is also summed at the same point. Full frequency control range, represented by a zero to +10 volts excursion at the input, becomes an offset -7.5 volts to -17.5 volts excursion at V_B, the output of the first inverting amplifier. The second inverting amplifier furnishes an equal but opposite voltage, V_A, exhibiting an excursion between +7.5 and +17.5 volts. The fixed voltages V_C and V_D are established as references. The subsequent section will utilize the terms (V_A - V_C) and (V_B - V_D) in converting to a zero current reference. Summation of V_C and V_D at the + input to the second inverting amplifier causes the terms (V_A - V_C) and (V_B - V_D) to track power supply variations proportionally.

In the following detailed analysis of the frequency control section refer to the schematic, figure 7-3. The setting of the main frequency control A1-R3 establishes a voltage at A1-TP1 between 0 and +10 volts. This voltage is calibrated by adjustable resistor A1-R1 for a midrange frequency. Other frequency ranges are calibrated by resistors A1-R4, A1-R6, and A1-R368. Resistive summing via A1-R7, A1-R9, and A1-R10 combines the main frequency control voltage with an offset derived from +12 volts, and with an external voltage when used in a voltage controlled generator (VCG) mode. Operational amplifiers A1-IC1 and A1-IC2 develop the negative control voltage V_B and the inverted positive control voltage V_A respectively. The range of operation of V_A is +7.5 to +17.5 volts, and V_B from -7.5 to -17.5 volts. A resistive divider network derives nominal ±7.5 volt reference voltages V_C and V_D from the ±12 volt power supplies. Potentiometer A1-R28 is employed as a symmetry adjustment for obtaining 50/50 duty cycle waveforms.

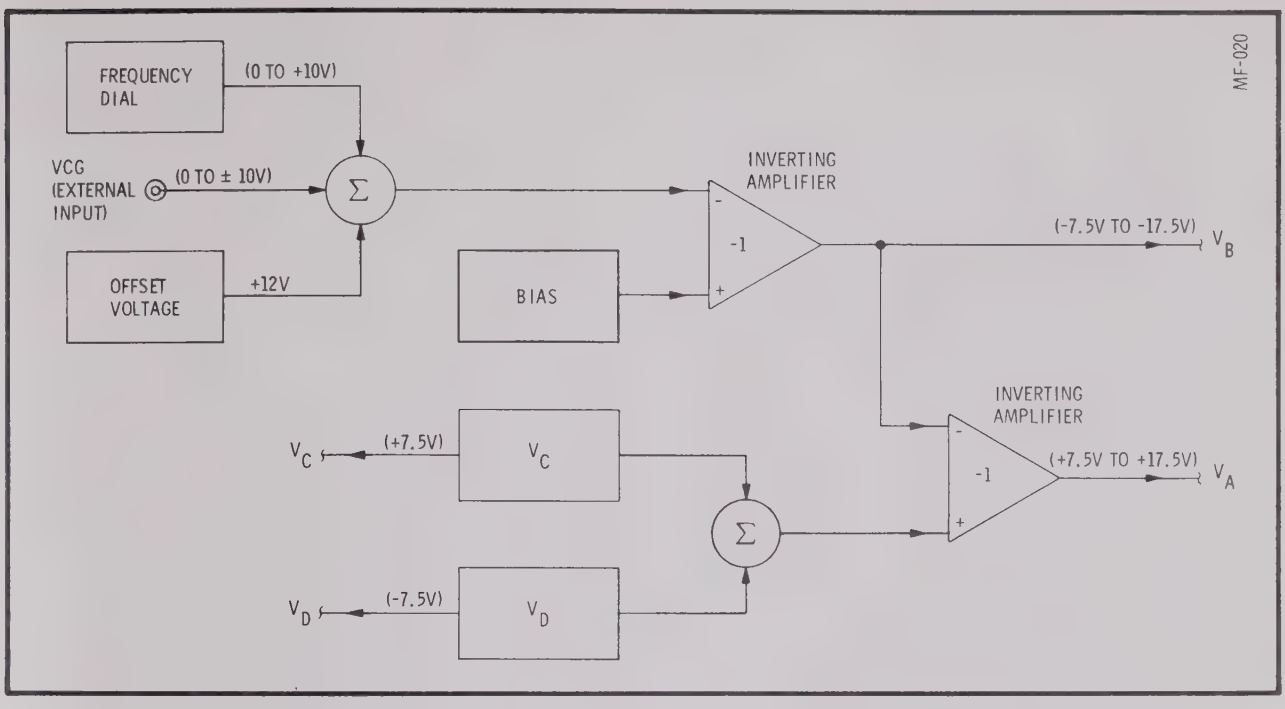


Figure 4-2. Frequency Control, Block Diagram

b. VOLTAGE-TO-CURRENT CONVERTER. - With reference to figure 4-3, the voltage difference terms (V_A - V_C) and (V_B - V_D) are impressed across the ramp and range resistive networks. The differencing is mechanized by means of operational amplifiers connected as voltage followers. Field effect transistors at the follower outputs serve to translate the voltages to currents i_A and i_B between the differing voltage levels at the follower and at the diode bridge current-steering switch. Alternate charging and discharging of the selectable integrating capacitors at the diode bridge output, under control of the squarewave, results in the desired triangular waveform.

The ramp and range networks are series-parallel combinations of resistors which determine the magnitude of currents i_A and i_B in accordance with control voltages (V_A - V_C) and (V_B - V_D), the selected frequency range and either a symmetrical 50/50 duty cycle or a 15/85 ramp. For 50/50 duty cycle operation, the series ramp network at V_A is shorted out, and the parallel network at V_B is opened. When a ramp function has been selected, the insertion of the series network reduced i_A by approximately 40 percent and the connection to the parallel network increases i_B to 333 percent. This satisifies the conditions necessary to generate the required voltage ramps at the integrating capacitors.

In the following detailed analysis of the voltage-to-current converter, refer to the schematic, figure 7-3. Voltages V_A and V_C are impressed across the MULTIPLIER switch network A1-R32 through A1-R40. The resultant current flow is dependent upon both the MULTIPLIER setting and WAVEFORM selection. Similarly, an opposite polarity current is developed by the network A1-R41 through A1-R49. The

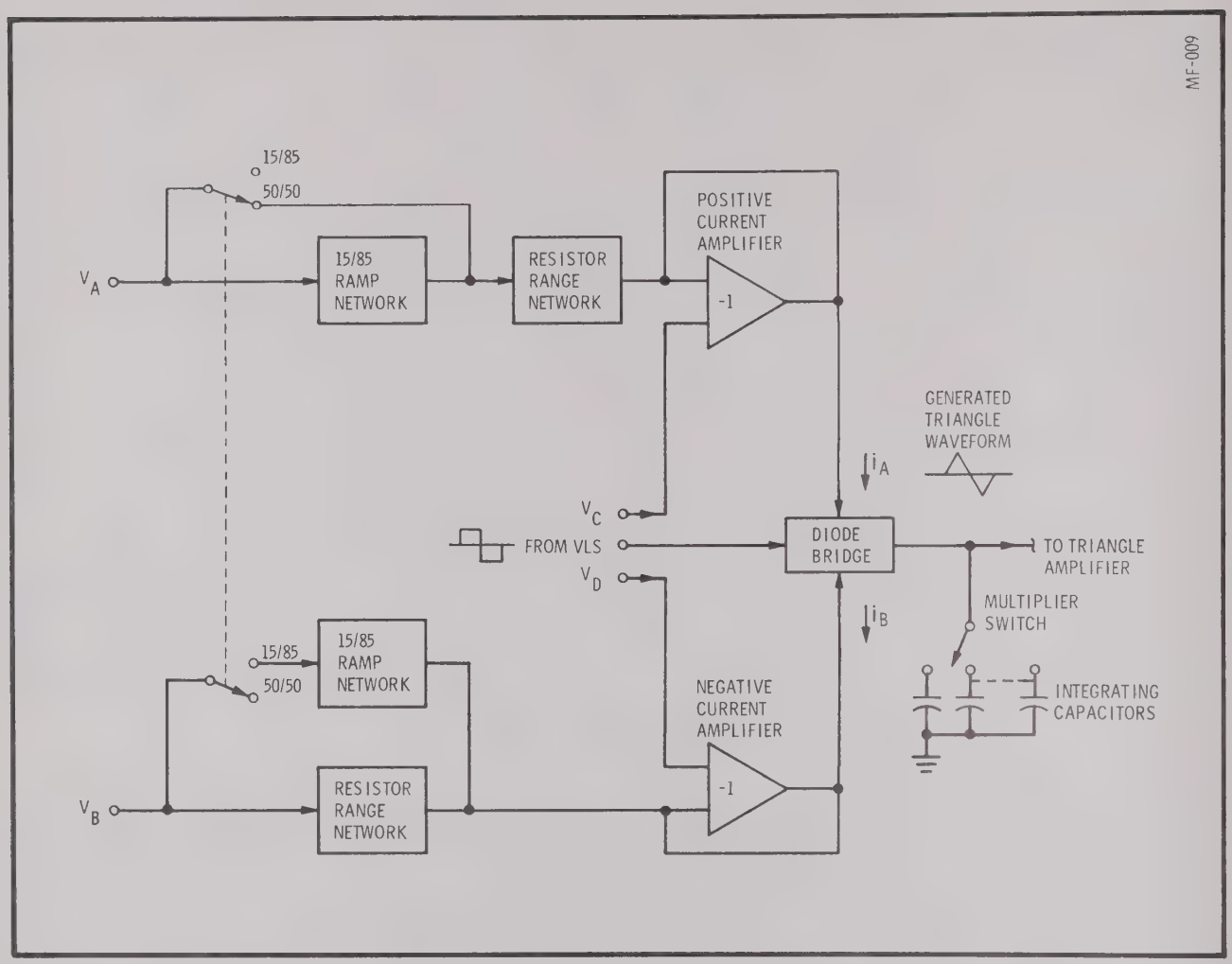


Figure 4-3. Voltage-To-Current Converter,Block Diagram

relationship between the two opposite polarity currents is modified by the WAVEFORM switch in accordance with the 15/85 duty cycle capability, by means of series network A1-R50, A1-R51, A1-R53 through A1-R57 and parallel network A1-R58 through A1-R65. When these networks are inserted, the resultant current from V_A is reduced to 50/85 of nominal, and the current from V_B is increased to 50/15 of nominal. The resultant integrator waveorm exhibits a 15/85 duty cycle, with negligivle shift of frequency fron the nominal 50/50 condition.

(1) Integrated circuit amplifiers A1-IC3 and A1-IC4 form the basis for active current sources. Because of the wide range of currents to be accommodated (approximately 2 na to 25 ma), field-effect buffers are required at input and output. The resultant performance approaches an ideal current source at

low frequencies (< 100 kHz) because of the high voltage gain of the amplifiers. At high frequencies (>100 kHz) the intrinsic output impedance of transistors A1-Q7 through A1-Q10 gives less perfect, but adequate, approximations to current source operation.

(2) Diodes A1-CR1 through A1-CR8 make up a current-steering bridge. When A1-TP7 is low (-3 volts), current will flow toward that test point from the upper (positive) current source. The lower (negative) current source will then accept current from the integrating capacitor through diodes A1-CR5 and A1-CR6. When A1-TP7 goes high (+3 volts), currents will interchange via the bridge. Note the use of two series diodes in each leg of the bridge. This is necessary because of the conflicting requirements of low leakage and low stored charge at extremes of the function generator frequency range. These characteristics are not obtainable to the required degree in a single diode.

(3) Integrating capacitors A1-C29 through A1-C34 are selected in accordance with the desired MULTIPLIER switch setting. The highest frequency range incorporates an adjustable capacitor for purposes of frequency calibration.

4-4. TRIANGLE AND INVERTER AMPLIFIERS

The triangle amplifier is a wideband, potentiometric, gain-of-four amplifier. Its purpose is to buffer the integrating capacitor as well as to furnish a low-impedance 6-volt p-p signal for succeeding circuitry. The inverting amplifier is of similar design, except that it is connected as a gain-of-minus-one amplifier to supply an inverted waveform with respect to the triangle amplifier output. The inverted waveform is utilized for reversed polarity ramp and pulse functions.

The block diagram, figure 4-4, indicates the input/output relationship of the triangle and inverter amplifier. The configuration is quite conventional. A major consideration is the potentiometric configuration of the triangle amplifier for obtaining extremely high input impedance. Not shown in the block diagram, but essential for the low-frequency ranges of the function generator, is the low-input-current, dual field-effect transistor A1-Q11.

a. TRIANGLE AMPLIFIER. - Field effect transistor A1-Q11 is connected as a source follower, driving the differential transistor array A1-IC5A. Because of the wideband requirements of the amplifier, A1-IC5 incorporates high-frequency transistors (f_T>1000 MHz). Again, in order to maintain wideband response, the output A1-IC5A is coupled through common-base amplifier A1-Q12 to the complementary emitter-follower output drivers A1-Q13 and A1-Q14. A1-Q65 provides a current source for the common base drive A1-Q12. The triangle monitor output is power boosted by the drivers A2-Q58 and A2-Q59. DC feedback is applied via A1-R91 and A1-R92, establishing a voltage gain of four with A1-R367 for calibration. High-frequency feedback is coupled with A1-C38, which is adjustable for purposes of shaping overall high-frequency response.

b. INVERTER AMPLIFIER. - Essentially identical design approach is employed as for the triangle amplifier, except that the inverter amplifier is simplified by elimination of the field-effect transistor input. The circuit shares one-half of array A1-IC5 and d-c biasing networks with the triangle amplifier. Feedback resistors A1-R105 and A1-R115 establish a nominal gain of minus one.

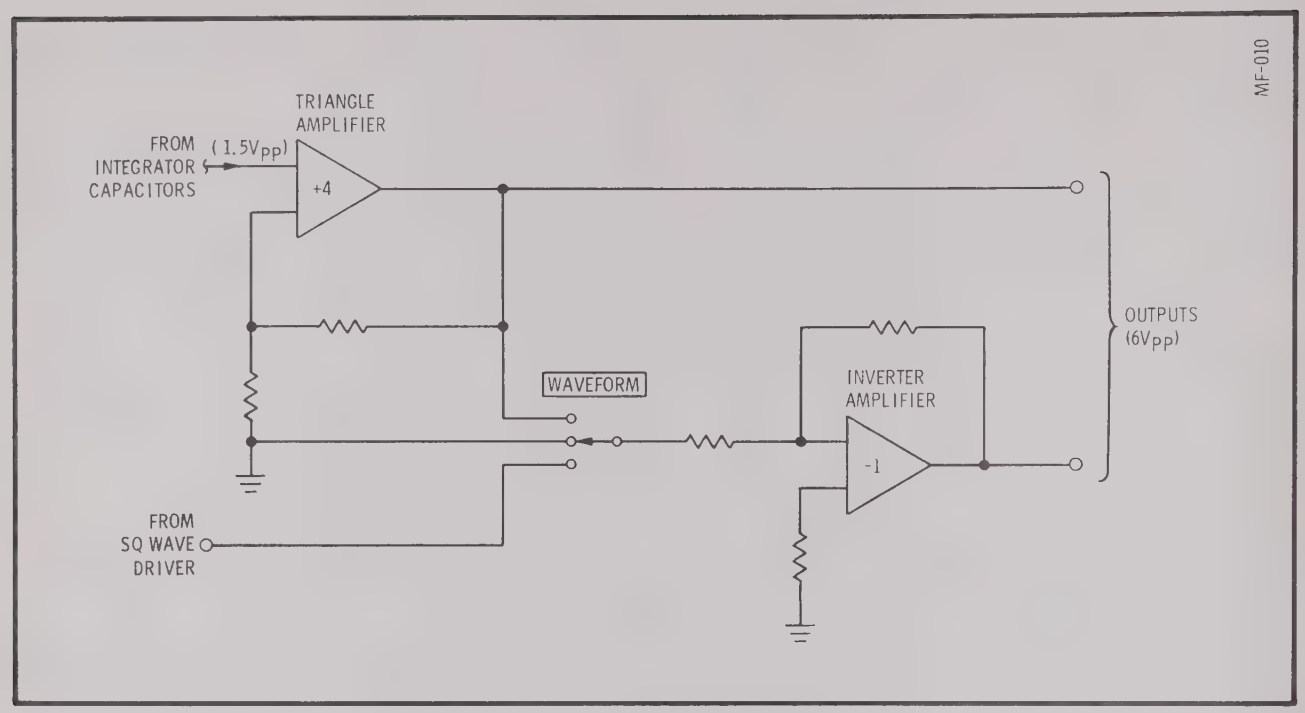


Figure 4-4. Triangle and Inverter Amplifier, Block Diagram

4-5 VOLTAGE LEVEL SENSOR AND AUTOMATIC LEVEL CONTROL OPERATION

The combined function of the VLS-ALC circuits is one of determining the point at which the main integrator ramp is caused to reverse slope. (Refer to the block diagrams, figures 4-5 and 4-6.) The VLS is essentially an ultra-fast comparator, referenced to a pair of adjustable d-c positive and negative reference levels.

The ALC is necessary on the highest frequency range only as a means for loop delay compensation. Together, the VLS and ALC form a peak amplitude regulator, with the error signal being the difference between a fixed d-c reference voltage and the peak (rectified) output of the triangle amplifier. In turn, the amplified error signal becomes a variable reference level to the VLS. Should the triangle amplifier peak amplitude vary from its established value, the resultant error signal will automatically cause the VLS comparison level to shift in the proper direction for a reduced error.

Note that the TRIGGER SYNC input signal also drives the VLS. Sync circuits provide for frequency-locking the function generator to an external source of sync pulses. Synchronization is achieved whenever a sync input pulse occurs within a period of 0 to -1 percent of the triangle peak. In essence, this implies that the sync pulse frequency (or a harmonic thereof) must be within 0 to +1 percent of the frequency established by the free-running function generator. The sync function is implemented by a transistor switch which causes a periodic reduction of 1 percent in the d-c reference level to the VLS.

a. VOLTAGE LEVEL SENSOR. - The VLS (figure 4-5), accepts a bidirectional ramp voltage waveform, and by means of two difference amplifiers, compares the input waveform against positive and negative reference levels. As the ramp input approaches V_R (+), the output current from the positive difference amplifier increases. When the positive tunnel-diode current reaches its characteristic "peak point" it will trigger on. The increased voltage drop across the on diode is coupled through an inverting driver to reset the current mode latch. (The reset condition of the latch is defined as a negative output voltage level with respect to ground.)

The bias feedback amplifier senses the state of the latch and feeds back conditioning levels to the tunnel diode circuits. The need for this feedback is dictated by the requirement for minimal recovery time.

As the input ramp approaches V_R (-), the output current from the negative difference amplifier increases, causing the negative tunnel diode to trigger on. An inverting driver in turn will set the current mode latch. The cycle is completed as the bias feedback amplifier again changes state in response to the toggling of the latch.

In the following more detailed discussion, refer to the schematic diagram, figure 7-3.

(1) DIFFERENCE AMPLIFIERS. - Transistor arrays A1-IC12 and A1-IC13 accept the integrator ramp waveform and reference levels V_R (+) and V_R(-). As the positive-going input voltage (A1-TP14) approaches V_R (+) (A1-TP17), there is an increased current flow at pin 12 of IC4. This current flow adds to the bias current of tunnel diode A1-CR40. When $e_{in} \approx V_R$ (+), total current will be sufficient to fire A1-CR40, causing an increased voltage drop across the diode. This voltage increase will be sufficient to turn on A1-Q51.

(2) CURRENT-MODE LATCH. - The transistor pair A1-Q53 and A1-Q54 forms a current-mode latch, so that the turn-off of A1-Q54 causes the turn-on of A1-Q53. As A1-Q54 turns off, its collector drops towards the -3 volt zener clamp level established by A1-CR54. The A1-Q54 collector level is coupled through driver transistors A1-R29, A1-Q57 and A1-Q58 to the VLS squarewave output A1-TP7.

(3) BIAS FEEDBACK AMPLIFIER. - Transistor pair A1-Q61 and A1-Q62 is a differential pair connected to provide a bias feedback function. When A1-Q54 goes off, it also turns off A1-Q62 (and turns on A1-Q61). The immediate effect is the reverse biasing of tunnel diode A1-CR40, and also causing tunnel diode A1-CR60 to be forward biased slightly below its firing current level. Potentiometer A1-R258 is provided to adjust the drive signal for optimum settling of the switched currents.

(4) RAMP REVERSAL. - Once diode A1-CR40 has fired, the input voltage ramp will reverse to become negative-going. As this ramp approaches V_R (-) A1-TP19, there is an increased current flow at pin 5 of A1-C13. This current flow adds to the bias current of tunnel diode A1-CR60. When $e_{in} \approx V_R$ (-), total current will be sufficient to fire A1-CR60. The firing of A1-CR60 will cause A1-Q60 to turn on, toward +12 volts. This rise of voltage is transmitted through A1-CR68 to reverse bias A1-Q53. Latch A1-Q53 and A1-Q54 reverses state, causing the output to change from -3 volts to +3 volts.

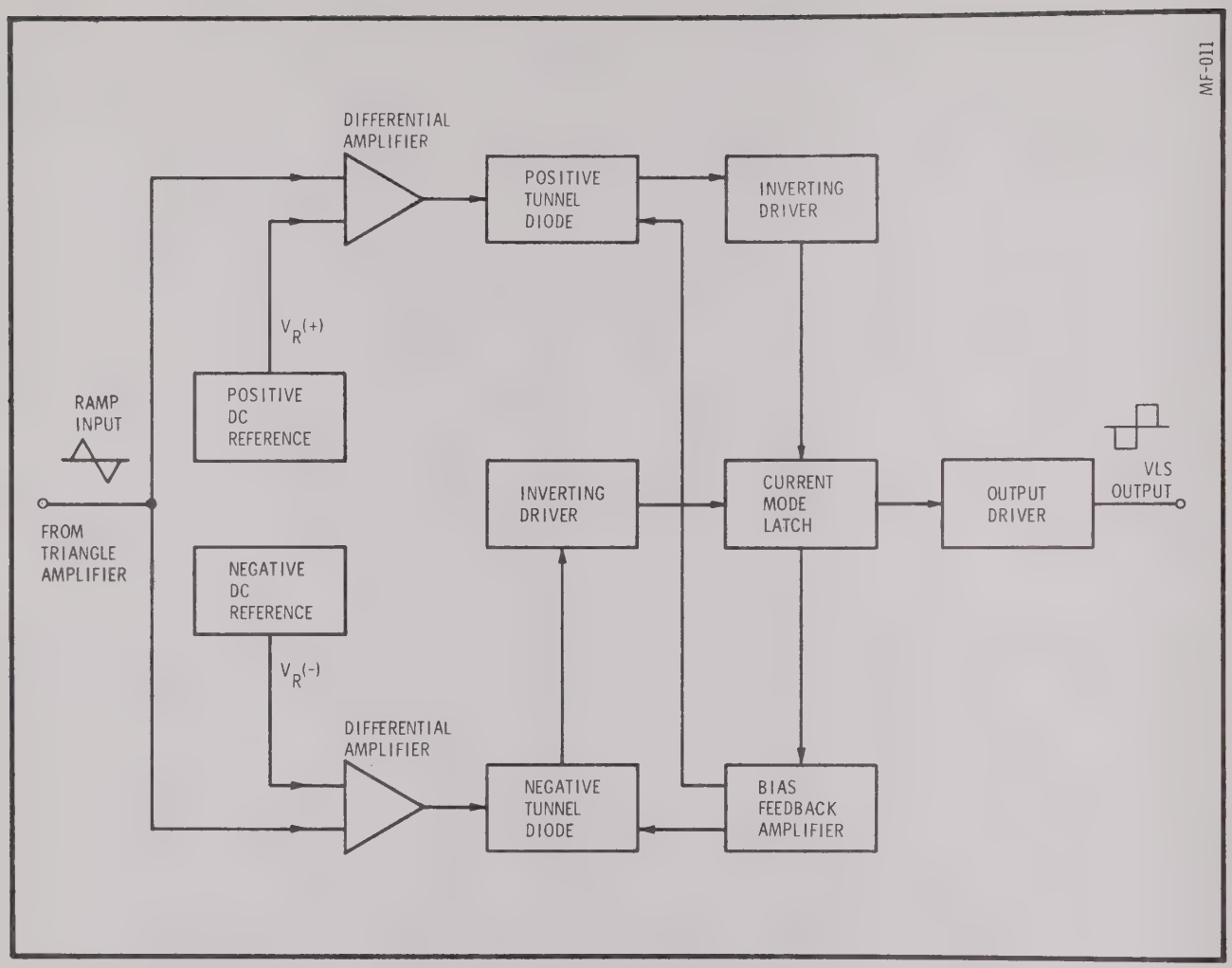


Figure 4-5. Voltage Level Sensor, Block Diagram

Following the reverse biasing of A1-Q53, bias current transfers from A1-Q61 to A1-Q62 in turn causing the reverse biasing of A1-CR60 and the partial forward biasing of A1-CR40.

At this point, the input ramp reverts to positive-going and the previously described sequence of events is repeated.

b. AUTOMATIC LEVEL CONTROL AND COMPENSATED LEVEL CONTROL. - The ALC is necessary on the highest frequency range only as a means for loop delay compensation. Without the ALC, the main loop performance would be severely limited at the high-frequency end because of the effect of propagation time around the loop (≈25 ns). Together, the VLS and ALC form a peak amplitude regulator, with the error signal being the difference between a fixed d-c reference voltage and the peak (rectified) output of the triangle amplifier. In turn, the amplifier error signal becomes a variable reference level to the VLS. If the triangle amplifier peak amplitude varies from its established value (because of integrator loop delay of ≈25 ns), the resultant error signal will automatically cause the VLS comparison level

to shift in the proper direction for a reduced error.

The primary ALC loop has the characteristic of a relatively long time constant, because of the need for rectifying and filtering of the control signal. The effect of this time constant is to degrade performance in response to fast VCG waveforms. The compensated level control (CLC) circuits are intended as a first order correction to overcome the effect of the ALC time constants. These circuits operate by deriving a linear approximation to the required delay compensation from control voltages V_A and V_B, as shown in figure 4-6.

Peak level detectors provide a means for comparing the actual peak ramp voltages against pre-established reference levels. The overall closed-loop operation is such that positive and negative peaks are independently regulated. Without the ALC, the VLS and main loop integrator delay totaling 25 ns would cause a 2 to 1 variation between 1 MHz and 10 MHz. With the ALC, amplitude variation due to delay becomes negligible, with second-order effects (such as peak detector inefficiency) becoming the limiting factors at the highest frequency.

In the following more detailed description, refer to the schematic diagram figure 7-3. The high-frequency ramp waveform, is peak-rectified via matched diodes A1-CR36 and A1-CR37. Operational amplifiers A1-IC9 and A1-IC11, connected as integrators, provide d-c gain. Selection between either the amplifier outputs or fixed d-c reference levels is made on the basis of frequency range. The complete ALC loop extends from the amplifier outputs to the VLS reference inputs, then to the main integrator, and back around to the peak detectors.

c. COMPENSATED LEVEL CONTROL. - The compensated level control amplifiers A1-IC10 and A1-IC14 are in series with ALC averaging amplifiers A1-IC9 and A1-IC11 respectively. In conjunction with resistive input networks, the amplifiers are adjustable for d-c control level and gain, thereby developing a first order correction for the loop delay. Note that, if this correction were perfect, there would be no need for the ALC circuits. However, becauses the correction is only approximate, the ALC supplies the necessary backup for maintaining accurate response in other than VCG or triggered modes. Interlocks through switches A1-S1, A1-S2, and A1-S3 provide for proper inspection of the level control circuits in accordance with selected modes and frequency ranges.

4-6. START/STOP AMPLIFIER

When in TRIG or GATE modes, the start/stop amplifier stops the operating of the main generator by inhibiting the triangle waveform. In these modes, the start/stop amplifier switches current from the integrating capacitor to the start/stop amplifier, thereby stopping generator oscillation.

The PHASE control determines the point at which the waveform is started and stopped. A1-R171 in a coarse adjustment trimmer for centering the PHASE control; if not properly adjusted A1-R171 can halt operation of the main generator.

Two logic inputs control start/stop amplifier operation; one from the voltage level sensor and one from trigger logic circuits (figure 7-3).

4-7. TRIGGER SYNC

The TRIGGER SYNC input circuit is simply a switch-controlled attenuator when used to synchronize the output. With reference to

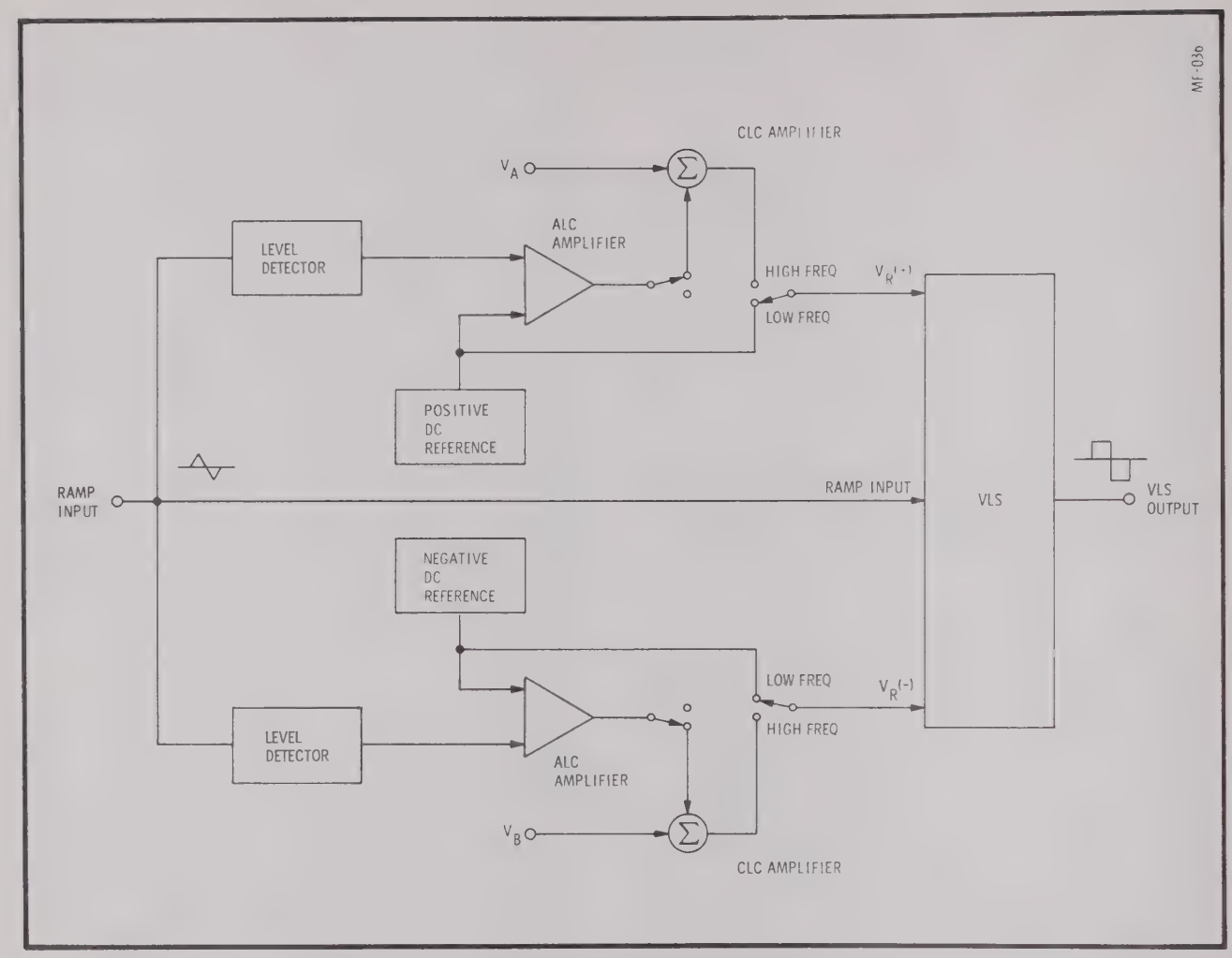


Figure 4-6. Automatic Level Control and Compensated Level Control, Block Diagram

figure 4-7, the presence of a pulse on the trigger sync input line will cause an attenuation of the VLS reference voltage V_R (+) or V_R (-). If this pulse coincides within 0 to -1 percent to the peak of the integrator ramp waveform, a reversal of the ramp will be forced. The net result, over the limited range of 0 to -1 percent, is the ability to cause the function generator to synchronize to an external train of pulses.

Either transistor A1-Q49 or A1-Q50 is driven on by the presence of a synchronizing pulse of 1 volt or more. A positive synchronizing pulse must coincide within limits to the positive ramp peak, and similarly for the negative pulse and peak. The resultant attenuation of the reference level to the VLS will force synchronization of the ramp to the pulse.

4-8. SINE SHAPER

The sinusoidal signal that is available as one of the functions generated by the function generator is produced by applying the triangular waveform of the main loop to a nonlinear network having an input-output relationship as shown in figure 4-8.

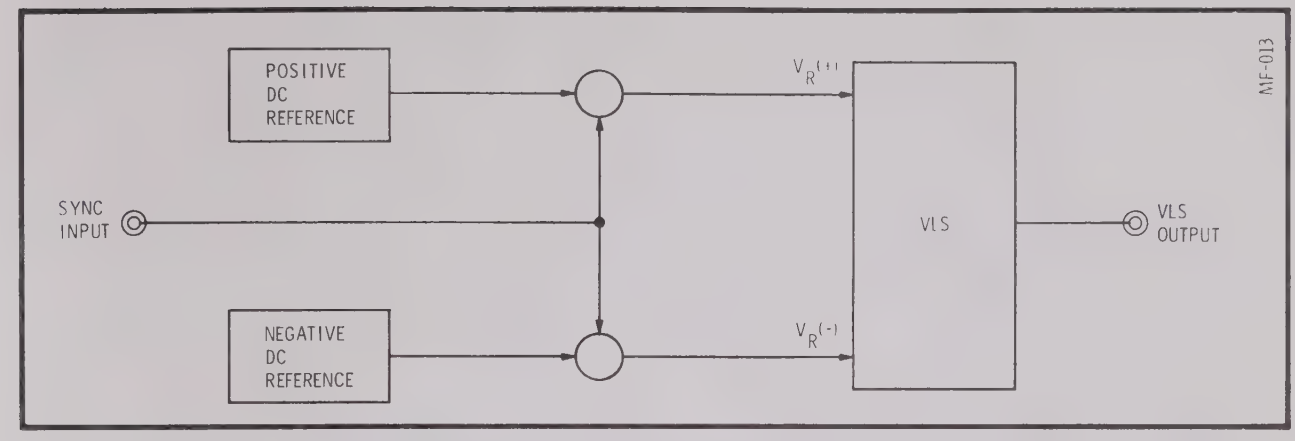


Figure 4-7. Sync Input, Block Diagram

The sine shaper block diagram is illustrated in figure 4-9. The triangular waveform driving the sine shaper has a peak-to-peak value of 6 volts.

Because of the sine-shaping process, the output peak value of the resulting sinewave will be approximately 3.8 volts peak-to-peak. In order to obtain a sinusoidal waveform on the same amplitude as the incoming triangular waveform, an amplifier is needed, with a gain of approximately 1.6.

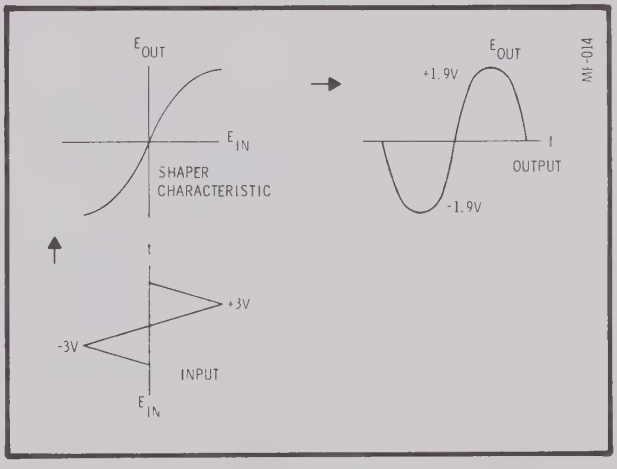


Figure 4-8. Sine Shaper Input/Output Diagram

The transfer characteristic shown in figure 4-8 is obtained by means of a network of resistors and voltage-controlled switches such that a nonlinear resistance is produced. The operation of this network is illustrated symbolically in figure 4-10. The diode switches in the figure represent transistors in the actual circuits. Each switch will conduct whenever the voltage at the ladder network point to which it is connected reaches the bias level of the point to which it is returned.

Consider the triangular waveform shown at the driver input. At zero volts, all switches are open, and the signal appears unchanged at output A. As the voltage increases in the positive direction, a point is reached where the voltage at node 1 is e_1, and switch S_1 closes. This clamps node 1 to voltage $+e_1$ volts. As the input voltage continues to rise, the voltage at node 2 eventually turns on S_2, clamping node 2 to voltage $+e_2$. This continues until the input reaches +3 volts, each successive switch clamping its corresponding node to a higher voltage. The net result is that the series string of resistors A2-R132 through A2-R137 presents an increasing load to the signal through A2-R129, and the output waveform bends smoothly in a close

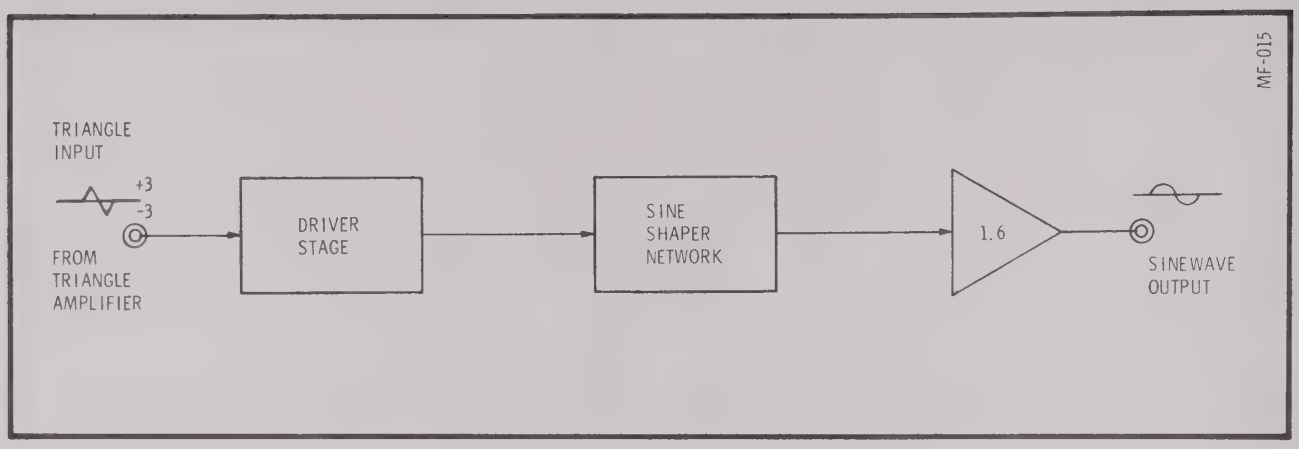


Figure 4-9. Sine Shaper, Block Diagram

simulation of a sinewave. The effect of switch S_7 is somewhat different. This switch closes just before the peak of the input triangle is reached, and its current passes through A2-R139 to ground. The voltage drop through A2-R139 generates the waveform shown at output point A. This is subtracted from the B signal by the differential amplifier to remove the remaining discontinuity at the peaks of the B waveform.

In the downward travel of the input signal, this action reverses, and switches S_7 through S_1 are opened one at a time as the switch bias voltages are reached. The negative portion of the cycle is now handled by switches $S1_1$ through $S1_7$ in a similar manner.

The clamping switches used in the actual circuit are emitter followers, with their bases accurately biased by a precision resistive network. This provides a low-impedance path to ground for the signal currents, and minimizes fluctuations in the bias voltages that might be caused by the flow of the signal currents through the bias resistors. As a result, the lower impedance network provides improved high frequency characteristics.

In the following detailed analysis of the sine shaper refer to the schematic, figure 7-5.

a. INPUT DRIVER. - This circuit comprises transistors A2-Q23, A2-Q24, A2-Q25, and A2-A26. The dual complementary emitter-follower arrangement results in cancellation of base-emitter function biases, good thermal characteristics, and an output impedance of approximately 10 ohms. Note that because of the nonlinear load presented by the sine shaper to this driver, the waveform seen at A2-TP31 will not be linear, but will show signs of increased loading toward the peaks; its peak-to-peak voltage will be approximately 3.8 volts when the input triangle at A2-TP28 is 6 volts peak-to-peak.

b. SINE SHAPER. - This section involves transistors A2-Q27 through A2-Q44. Emitter follower A2-Q27 sets the positive voltage at the top of the resistive bias network A2-RN1. This voltage ia adjusted by means of pot A2-R127. The foot of the ladder network is biased by means of emitter-follower A2-Q35. Both A2-Q27 and A2-Q35 are npn transistors, so that any temperature changes will cause the top and foot of the ladder network to shift

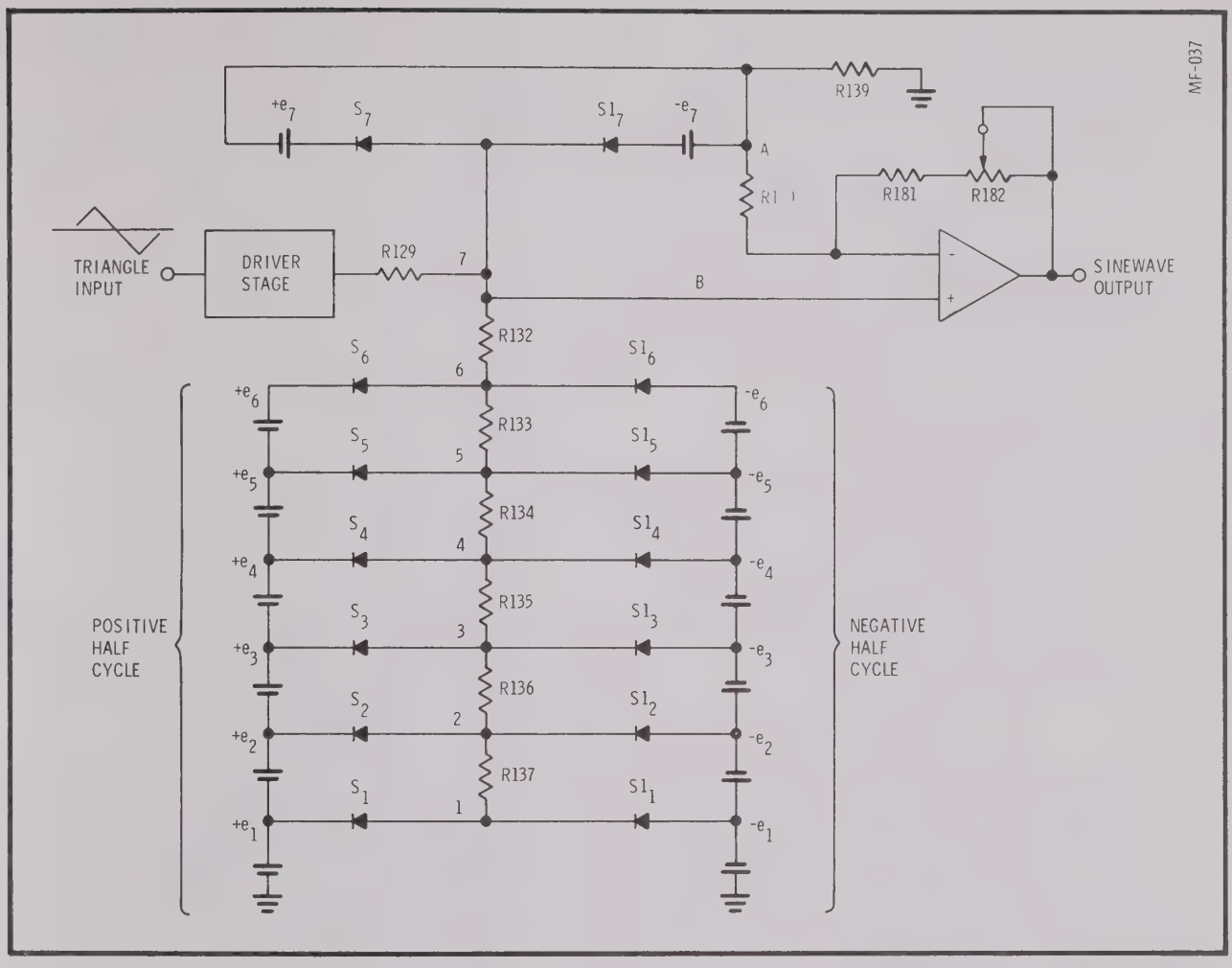


Figure 4-10. Sine Shaper Network

together in voltage. This provides temperature compensation to all clamp emitter-followers biased by the ladder.

Transistors A2-Q28 through A2-Q34 do the clamping for the positive half-cycle of the waveform. Each base is biased to a voltage 0.6 volt lower that the desired clamping level. Resistors A2-R132 through A2-R137 form the loading network for the driving resistor A2-R129.

The circuitry on the right side (A2-Q36 to A2-Q42) is a mirror image of the section just described, and performs the same function for the negative half of the cycle. The partly-shaped waveform can be observed at A2-TP31. The peaks will still be pointed, however, because the peak cancellation transistors A2-Q28 and A2-Q36 operate on the waveform by means of the subtraction operation performed by the sine amplifier.

c. SINE AMPLIFIER. - The sine amplifier (comprising transistors A2-Q53 through A2-Q57) is of similar design to the triangle amplifier and inverter amplifier. The sine amplifier,

like the triangle amplifier, is configured in the potentiometric mode. Overall gain with feedback is nominally +1.6. At the input to the amplifier, filter components A2-L3 and A2-C43 attenuate noise and distortion at frequencies above 10 MHz. The peak of the triangle waveform is cancelled by a signal across A2-R130, to the inverting input of the sine amplifier.

4-9. VARIABLE PULSE

The variable pulse circuits provide a means for obtaining an output pulse, variable between 5 percent and 95 percent duty cycle, at a repetition rate established by the frequency setting of the function generator. The variable pulse can also be modulated from an external ±10 volt source (PWM input).

Figure 4-11 shows the method of developing the variable width pulse.. At some variable point during the ramp cycle, the sum of the instantaneous ramp voltage and the d-c output of the pulse width control will be zero. This point can occur anywhere within the extremes of the ramp. The output pulse will be a rectangular wave, with transistions at the two points on the ramp where the summed voltages are equal to zero.

As shown on the detailed schematic, figure 7-5, comparator A2-IC1 generates a positive-going pulse whenever the ramp voltage at A2-R27 is more positive than the variable d-c level at A2-R26. Feedback network A2-R31 and A2-R32 provides a small amount of positive feedback to ensure a clean transition. The comparator output is coupled to a current-mode driver (A2-Q10 and A2-Q11). The output of A2-Q11, clamped at ±5 volts, is buffered by a pair of complementary emitter follower drivers.

4-10. SUMMING AMPLIFIER AND OUTPUT AMPLIFIER

The output stages are designed in two sections. The first section is an inverting summing amplifier with multiple purposes:

- Introduces fixed offsets to obtain zero-based waveforms
- Attenuates signal 6 db in fixed offset modes
- Provides a low impedance drive to a calibrated attenuator

The output section amplifies the signal from the attenuator to the voltage and power level needed for rated output. This amplifier operates as a (noninverting) potentiometric amplifier with inherently high input impedance. The attenuation is thereby unaffected by amplifier loading. The closed loop gain of the amplifier is nominally +5, which is adequate to ensure a 30-volt p-p output (open circuit) capability from internal signal sources.

Figures 4-12, 7-3, and 7-5 show the components of the output amplifier and its controls. Note that five front panel controls are associated with its operation; they are:

- WAVEFORM selector switch (A1-S2-4)
- OFFSET switch (A2-S1)
- OFFSET ADJUST control (A2-R4)
- OUTPUT ADJUST control (A2-R124)
- ATTENUATOR switch (A1-S3)

The output waveform, which may be one of several selectable by means of the WAVEFORM switch, can be amplitude controlled by either the step attenuator or the continuous OUTPUT ADJUST control. The step attenuator

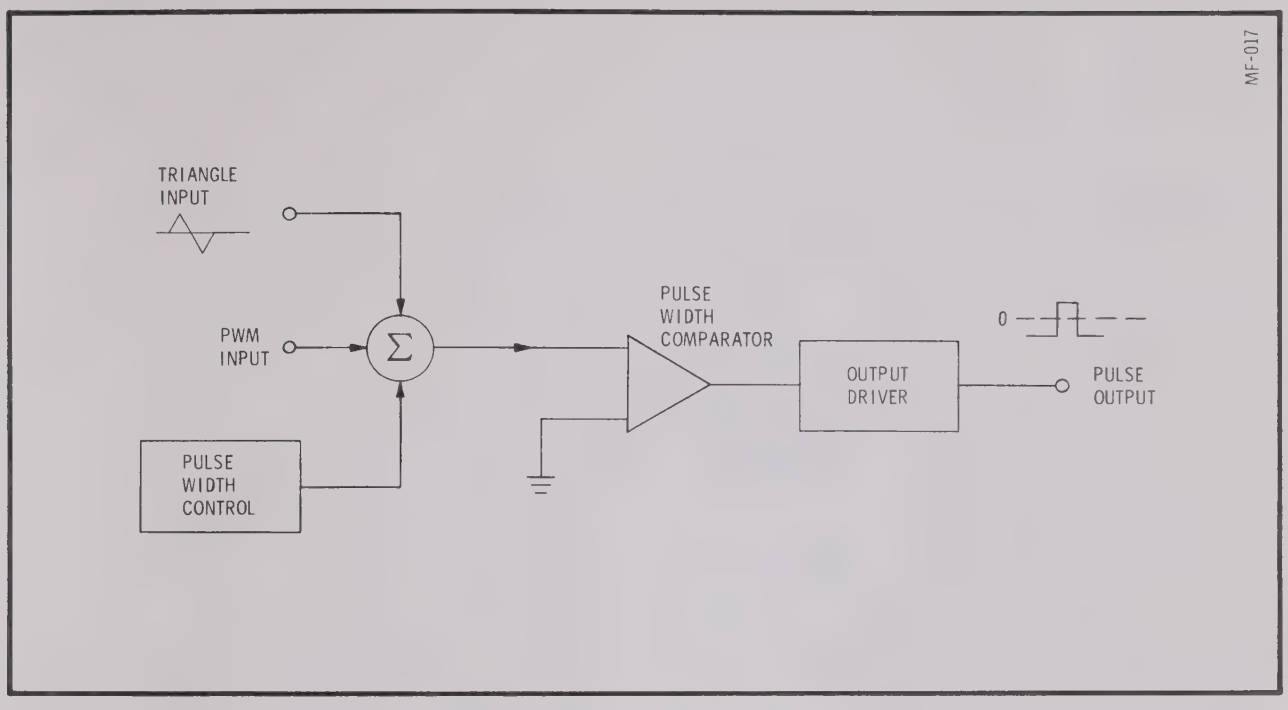


Figure 4-11. Variable Pulse Width, Block Diagram

provides seven accurate attenuation steps from the maximum output signal of 30 volts peak-to-peak. With the OUTPUT ADJUST control set to the CAL position (fully clockwise), the output levels obtained by rotating the step attenuator will be as follows:

		50-Ohm Load
1st Position	No Attenuation	15 volts p-p output
2nd Position	0 db Ref. level	10 volts p-p output
3rd Position	-10 db	3.16 volts p-p output
4th Position	-20 db	1.0 volt p-p output
5th Position	-30 db	0.316 volt p-p output
6th Position	-40 db	0.1 volt p-p output
7th Position	-50 db	0.0316 volt p-p output

For each position of the step attenuator, the variable OUTPUT ADJUST control provides and additional 20 db of continuous attenuation.

The step attenuator is divided into two sections. The first, using a single switch pole, operates between the two amplifier states and performs the attenuation for the -3 db from MAX to 0 db positions. The second section inserts 50-ohm pads at the output to provide the -10 db, -20 db, -30 db, -40 db, and -50 db overall attenuation steps.

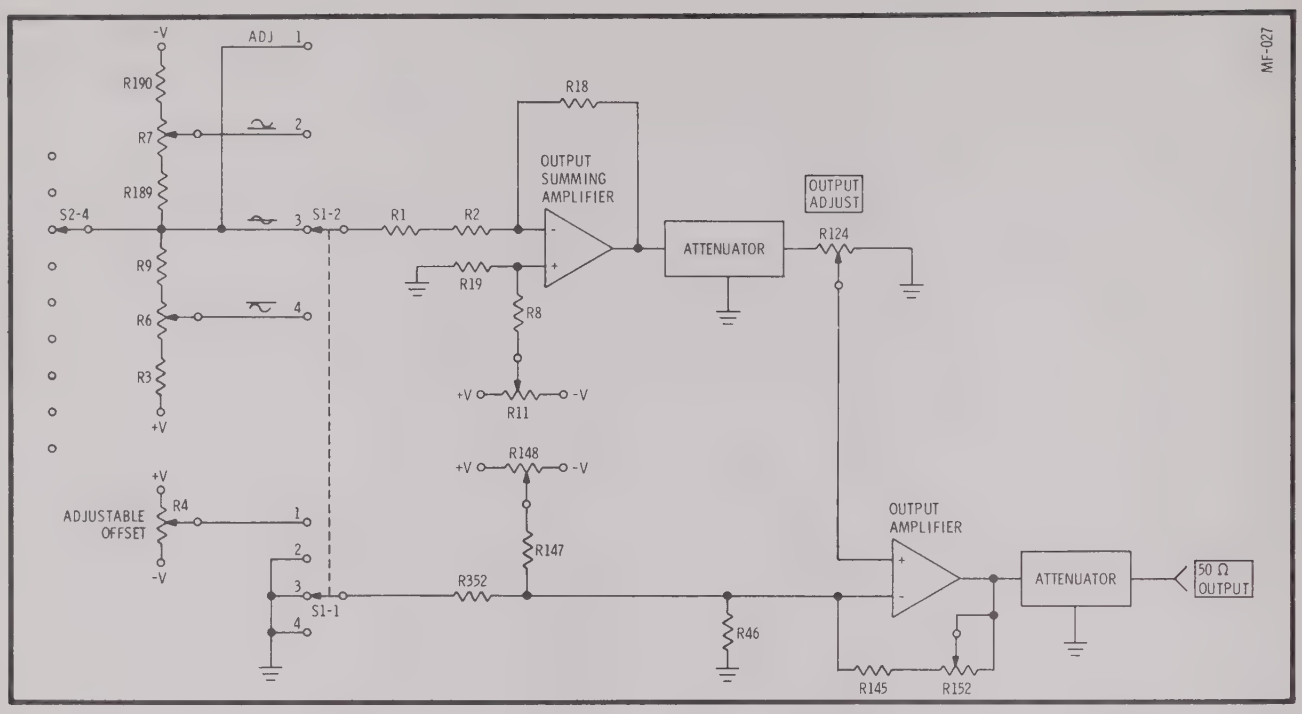


Figure 4-12. Output Amplifier, Block Diagram

The output stage gain can be adjusted by means of the variable resistor A1-R152 in its feedback path. The correct setting for this adjustment is such that the maximum output voltage into a 50-ohm load is 15 volts p-p, and corresponds very nearly to an amplifier gain of +5.

The second section of the attenuator operates at the output terminal. It introduces no attenuation in positions 1 and 2 of the attenuator, because in these positions the signal reduction is provided by the interstage attenuator. In the next five positions of the switch, the second section progressively inserts a -10 db, a -20 db, and a -30 db pad in the output signal path, and then adds attenuator pads in series to obtain -40 and -50 db attenuation. Most of the attenuation is at the output terminal to ensure a good signal-to-noise performance ratio.

Attenuator Position	Interstage Section	Output Section
1st: 15 volts p-p	No attenuation	No attenuation
2nd: 0 db Ref. (10 volts p-p)	-3.52 db	No attenuation
3rd: -10 db	-3.52 db	-10 db
4th: -20 db	-3.52 db	-20 db
5th: -30 db	-3.52 db	-30 db
6th: -40 db	-3.52 db	-40 db
7th: -50 db	-3.52 db	-50 db

The Interstate attenuator consists of a resistive divider comprising resistors A2-R122 and A2-R124.

The output amplifier signal is fed to the 50-ohm load through A1-R159 and A1-R160 (50 ohms) in the first two attenuator positions from 15 volts p-p to 0 db, the 10-volt reference. The resistive attenuator pads that are inserted in the next five positions are symmetrical 50-ohm pads. They are so designed as to minimize the resistor values used in order to reduce the effects of stray capacitance on the waveform . The first is a -10 db section (A1-R159 through A1-R163). The second is a -20 db T section (A1-R345, A1-R346, A1-R347). The third is a -30 db pad using four components (A1-R348 through A1-R351). The fourth and fifth are seried attenuator pads.

In the following detailed description, refer to figure 4-12 and schematic figure 7-5.

a. WAVEFORM AND OFFSET SWITCHES. - The input signal that drives the summing amplifier is derived from the wiper arm of the WAVEFORM switch (A1-S2-4), where one of eight possible waveforms may be selected. Each of these waveforms comes from a source whose equivalent circuit consists of a 6-volt p-p generator with an internal impedance of 100 ohms. The signal is fed to the summing amplifier input resistor (A2-R1). Additional inputs to the summing amplifier are derived from the OFFSET switch (A1-S3), providing for fixed modes. The fixed offset level is resistor-summed with the input signal which also attenuates the signal by 6 db. The adjustable offset is introduced into the final output amplifier at the inverting input by switching in a variable d-c level by A2-R4.

b. SUMMING AMPLIFIER. - The summing amplifier is configured as an inverting amplifier with an overall gain of -1. Differential pair A2-Q1 and A2-Q2 is a common emitter pair, with the overall amplifier summing function at the base of A2-Q1. Common base amplifier A2-Q5 provides voltage gain, and high frequency amplifier A2-Q6 assists in obtaining wideband response. Output emitter follower A2-Q7 and A2-Q8 provide the necessary low impedance for driving the attenuator network and OUTPUT ADJUST control.

c. OUTPUT AMPLIFIER. - The signal from the OUTPUT ADJUST control is fed directly to input transistor A1-Q18. Differential pair A1-Q19 and A1-Q20 is a common emitter pair amplifier, with overall amplifier feedback applied to base of A1-Q42. Transistors A1-Q44 and A1-Q18 serve as current sources to bias the common base output drivers A1-Q21 and A1-Q22. Current sources A1-Q44 and A1-Q18 are also driven at high frequencies through A1-C45 and A1-C44, thereby extending high frequency performance by an order of magnitude. Cascaded emitter followers A1-Q23 through A1-Q26 provide necessary power gain to supply the amplifier load.

4-11. TRIGGER LOGIC CONTROL

Operational modes, involving the use of an external trigger, utilize the differential comparator A2-IC2. The input signal is summed with a d-c potential derived from the TRIGGER LEVEL control. This control allows a point of an input waveform to be used as a trigger level. The output of the comparator is buffered and inverted by A2-IC3A and A2-IC3B. The TRIG SLOPE pushbutton selects either a positive or a negative slope to be used as a trigger.

The MAN pushbutton allows internal trigger operation without need of an external trigger connection.

When the MAN pushbutton is depressed, A2-IC3C and A2-IC3B form a lock-up circuit which prevents multiple triggering that may occur from switch contact bounce.

A2-IC3 through A2-IC7 are NAND gates which have the logic characteristics shown in the truth table, figure 4-13. Refer to the control logic timing diagrams in table 5-10 and to the schematic diagram, figure 7-5, for the following description.

a. TRIGGER MODE. - In TRIG MODE an external trigger or manual pushbutton forces A2-TP7 high and A2-TP8 low. When A2-TP8 goes low, A2-TP9 follows low and the d-c logic signal to the start/stop amplifier goes low, unlocking the waveform generating loop and allowing the waveform generator to begin. The start/stop amplifier may be released for operation by either the logic signal just described going low, or by a squarewave logic signal derived directly from the VLS going low, or both. In standby, the VLS logic signal is stalled high so the waveform commences as a result of A2-TP9 going low.

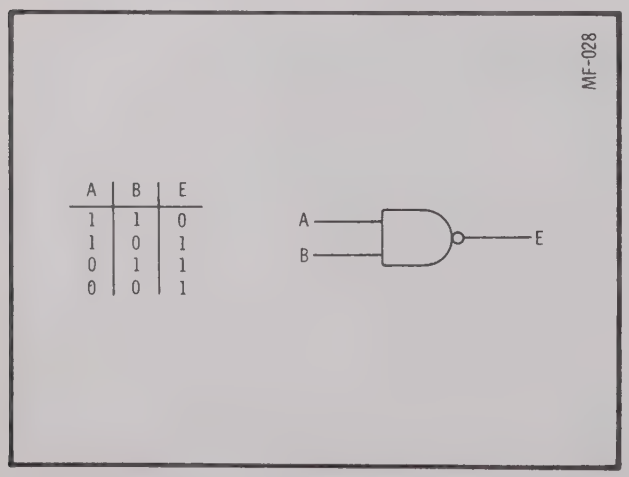


Figure 4-13. NAND Logic

As A2-TP9 goes low, A2-IC4B pin 6 is forced low; A2-TP6 goes low; A2-IC4A pin 2 goes low and A2-TP8 goes high. Thus, regardless of how long external trigger A2-TP7 remains high, A2-TP8 is reset as soon as A2-TP9 is latched. Another trigger cycle cannot occur until A2-TP7 is allowed to go low, resetting A2-TP6 high and re-establishing the initial conditions.

Conditions required for removing the operate command A2-TP9 from the waveform generator are:

(1) VLS waveform must be positive at A2-IC4D pin 13.

(2) A2-TP8 must be positive (indicating trigger reset).

(3) A2-IC5B pin 7 must be positive (indicating a logic GO command).

When these three conditions are present, A2-IC4D pin 14 goes low, setting flip-flop output A2-TP10 low.

At this time, A2-IC5C pin 9 (the logic run flip-flop reset line) is high because the VLS waveform is high. When the VLS waveform goes low (because of the main loop oscillator waveform reversing slope), A2-IC5C pin 9 will go low and reset A2-TP9 to initial conditions. The start/stop amplifier still commands waveform generation; however, because the VLS waveform also enters a start/stop amplifier, it holds the run command until the VLS waveform again goes positive.

b. GATE MODE. - The GATE MODE operates exactly as described for trigger mode except that the line A2-IC4A pin 2 is held high at all times. This holds A2-TP8 low for the entire time that a trigger signal A2-TP7 is present (high). When A2-TP7 goes low the generator completes its cycle and stops.

c. CONTINUOUS MODE. - In CONT MODE, the start/stop amplifier is forced into a run mode by grounding the logic line at the CONT MODE switch.

A2-IC4A pin 2 is similarly grounded and prevents A2-TP8 from being operated by any external conditions.

The external TRIGGER SYNC input is rerouted to the main loop sync circuit allowing external signals to force waveform transitions and thus provide a range of waveform sync lock.

d. PHASE-LOCK MODE.‡ - In ϕ LOCK mode an external trigger forces A2-TP9 low, (as in normal trigger mode), and an internal trigger derived from VLS waveform, forces A2-TP7 to reset high. The reset requirement is slightly different than trigger mode operation in that once reset, the reset signal A2-IC5 pin 9 must disappear quickly to allow acceptance of another trigger. A2-IC6 has been added to provide the same capability for the VLS waveform that A2-IC7B and C provides for the trigger signal.‡

IC5 pin 7 is set low in a trigger mode operation: A2-TP7 goes high and A2-TP9 goes low; A2-TP9 goes low, and A2-TP2 resets high.‡

With A2-TP9 low, A2-IC5 pin 7 and A2-IC5 pin 6 are high. Flip-flop A2-TP12 is forced high by the VLS waveform (free running) being high (A2-IC6 pin 13); (A2-TP11) is low.‡

When the VLS waveform goes low, A2-TP12 goes high and gate output A2-TP14 goes low resetting A2-TP9 high and A2-IC5 pin 7 low. A2-IC5B pin 7 goes low, resets A2-TP12 high and forces A2-TP14 high, thus completing the reset cycle of A2-TP9 and clearing the flip-flop A2-IC5B and C for a new trigger.‡

Flip-flop A2-IC5B and A2-IC5C thus form a digital phase detector with transitions in one direction forced by the external input trigger, and transitions in the other direction forced by the waveform generator. If these transitions are equally spaced, a timed symmetrical wave will be produced which indicates a fundamental phase lock at 180 degrees. As the symmetry varies, indications up to ±180 degrees from this point may be observed. This is detected by d-c averaging the waveform in the phase-lock circuitry.‡

An additional A2-IC7 has been added to indicate (by means of a lamp) when the waveform generator is phase locked at the same frequency as an external trigger frequency. This is explained in a logical order as follows:‡

(1) The positive edge of an incoming trigger causes A2-IC5 pin 7 to go high. Because A2-TP7 is differentiated, the pulse so produced disappears before A2-IC5B pin 7 goes high and no negative edge will be produced at A2-TP16. If however, an A2-TP7 pulse occurs while A-IC5B pin 7 is already high, a sharp negative-going pulse will occur at A2-TP16. This indicates either a plurality of pulses on the A2-TP7 line, or that the input trigger frequency is above the waveform generator frequency.‡

‡The Model F52 does not provide the phase-lock feature.

(2) A similar action in gate A2-IC7B indicates, by negative-going pulses, when the input trigger frequency is below the waveform generator frequency.‡

(3) A negative pulse on either gate A2-TP15 or gate A2-TP16 initiates a one-shot circuit. A2-IC7 pin 3 is forced low by the spike; the lamp transistor A2-Q14 is released; the lamp goes out, and timing capacitor A2-C20 begins to charge in a positive direction. When a sufficiently positive potential is achieved, unijunction transistor A2-Q15 fires and transistor A2-Q16 conducts, causing A2-IC7 pin 3 to go high A2-Q14 conducts , and capacitor A2-C14 is discharged through A2-Q14 and A2-Q15. When another negative pulse is received, the process is repeated.‡

4-12. PHASE-LOCK CONTROL ‡

The function generator can be phase-locked to an external signal injected at the TRIGGER SYNC terminal, with the ϕ LOCK pushbutton depressed. Under these conditions, the function generator output signal frequency will be identical to the input signal frequency, and will track this signal over a range equal to that of the frequency dial setting. Further, it can be made to track any harmonic (up to at least the fifth) of the input signal, or any subharmonic (down to at least the fifth). The input signal may be a sine, triangle, or squarewave, or a train of pulses. The phase, or time, relationship between output and input can be continuously adjusted to nearly one-half a period of the highest frequency signal. This amounts to ±180 degrees when the fundamental is being tracked.‡

The block diagram of figure 4-14 shows the basic elements of the loop. Note that the block labeled VOLTAGE CONTROLLED GENERATOR (VCG) represents the main waveform generating circuitry. This circuitry comprises the current control circuits, triangle generator, and level sensors. The circuitry generates the function generator waveform that is to be phase-locked to the input signal, and whose frequency can be changed by means of a control voltage applied to its input.‡

The input signal is first passed through a comparator stage where it is voltage-limited to provide an accurate determination of the zero-crossing points of the input waveform. Switch A2-S3-3 (TRIG SLOPE pushbutton on front panel) permits the operator to select a signal either in phase with the input or 180 degrees out of phase with the input, for use at the digital phase detector.‡

These, then, are preliminary wave-shaping functions, and are not directly related to the actual loop operation.

The digital phase detector is a set/reset flip-flop which is set by the input waveform at S and reset by the VCG signal at R as shown in the block diagram, figure 4-14. Assuming that these two signals are of equal frequency and 180 degrees apart, the resulting waveform at the phase detector output will be a squarewave (50 percent duty cycle). The duty cycle of the output waveform will deviate from 50 percent if the phase angle between the S and R input signals deviates from 180 degrees, as shown in figure 4-15.‡

The positive-going edges of the S and R signals are shown in heavy lines (figure 4-15) to illustrate the fact that it is these transitions which trigger the flip-flop into a change of

‡The Model F52 does not provide the phase-lock feature.

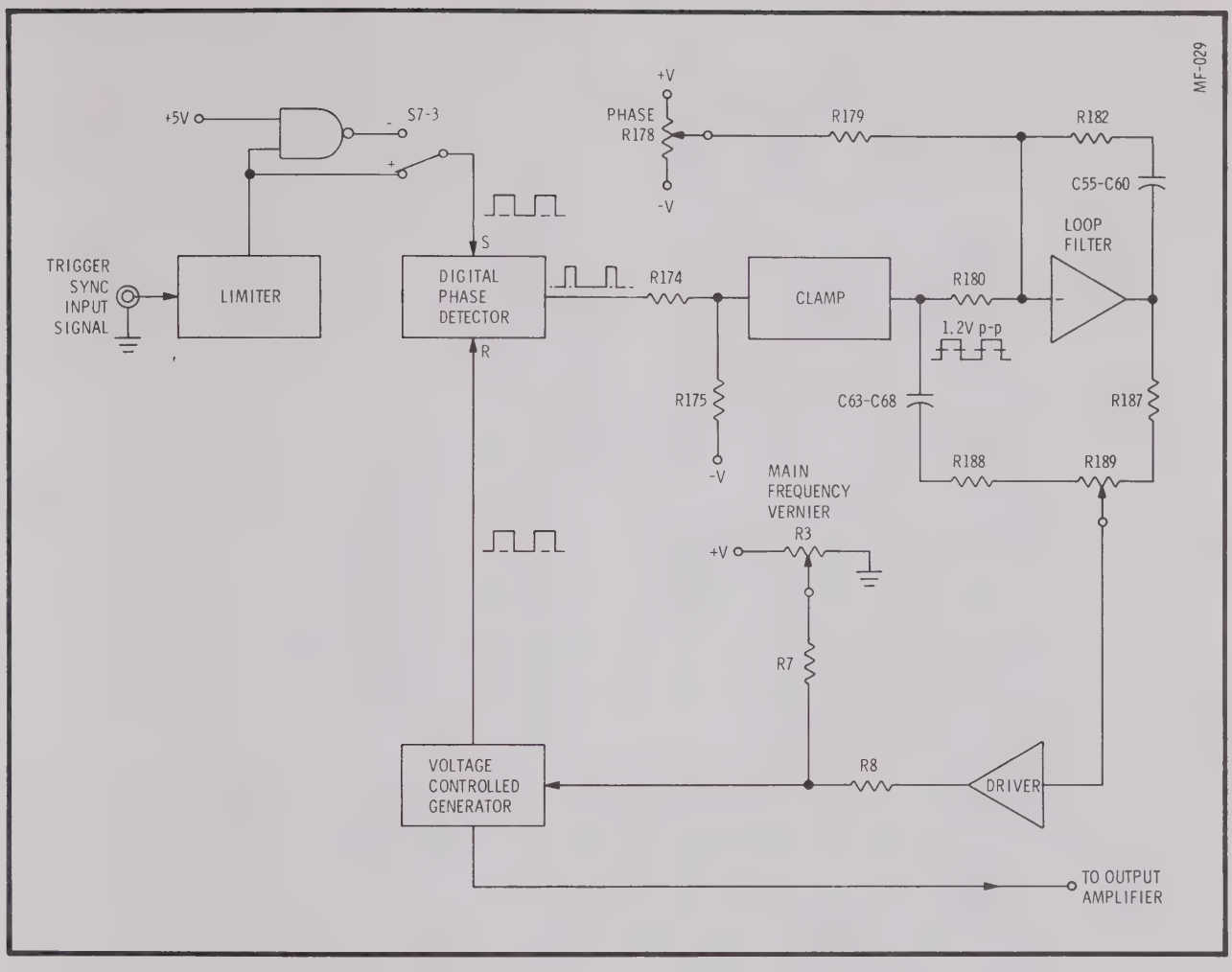


Figure 4-14. Phase-Lock Loop, Block Diagram

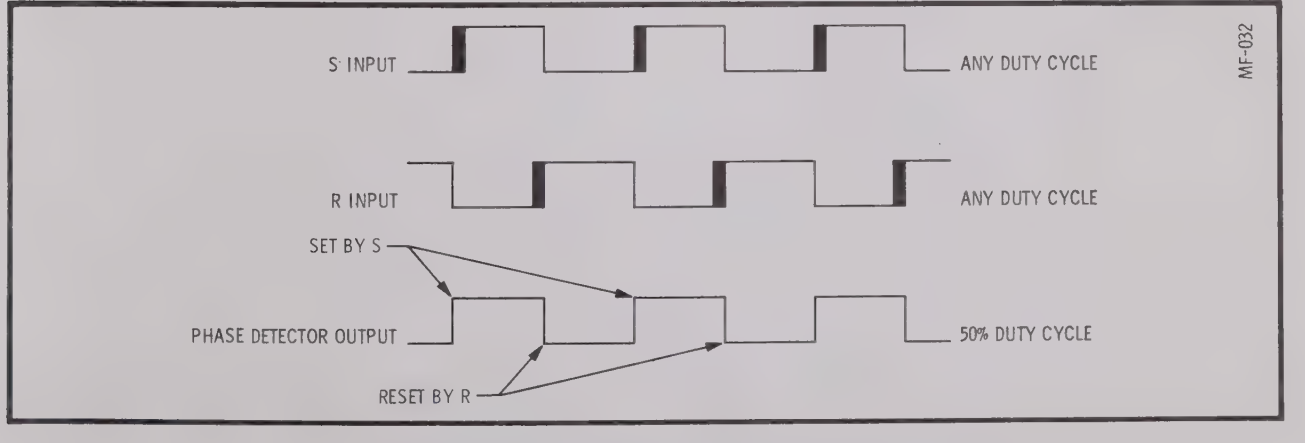


Figure 4-15. Phase Detector Waveforms for $\phi = 180°$

state. Because the negative-going transitions have no effect, the duty cycle of the input signals is irrelevant, and the phase angle between the S and R signals is defined strictly in terms of the positive-going edges. If the phase angle is less than 180 degrees, the duty cycle at the output will be less than 50 percent. Figure 4-16 shows these waveforms.‡

Thus, a net d-c voltage change will appear at the output which is a linear function of the phase angle of the input signals over a range of ±180 degrees.‡

Integrated circuit TTL devices are used in the digital phase detector and, as a result, the output waveform swings between zero and approximately +2.4 volts. A negative voltage is added to this signal and the result is applied to a diode clamp to obtain a signal which is symmetrical about zero. In this way, a signal of ±0.6 volt is obtained, and its net d-c voltage is zero when the duty cycle is 50 percent (corresponding to 180 degree input phase angle). Integration of this signal by an active integrator produces the d-c voltage which is used to control the VCG signal frequency that closes the loop at the R input of the phase detector.‡.

The integrator, as shown in figure 4-14, is shunted by the network composed of A1-C63 through A1-C68 and A1-R188 in series, so that two signals are added at the arm of potentiometer A1-R189. The signal at the output of the integrator contains the d-c voltage obtained by integration over the past history of the input signal, and also some a-c signal equal to the input signal times the ratio A1-R182:A1-R180. A1-R182 cannot be made equal to zero because the loop would then be completely undamped, and in this case, unstable. But, by adding the a-c component of the input signal in phase opposition with the output, and using the proper time constant in the cancellation path, this ripple signal can be almost completely eliminated. If this cancellation is not effected, the output ripple will modulate the VCG in such a way that its output signal duty cycle will not be 50 percent when the lop is closed.‡

The capacitors in the active integrator circuit are connected to the MULTIPLIER switch, so that their values change in sync with frequency range changes at the MULTIPLIER switch.‡

In the ϕ LOCK mode, fundamental frequencies can be tracked from 10 Hz to 10MHz. Harmonics

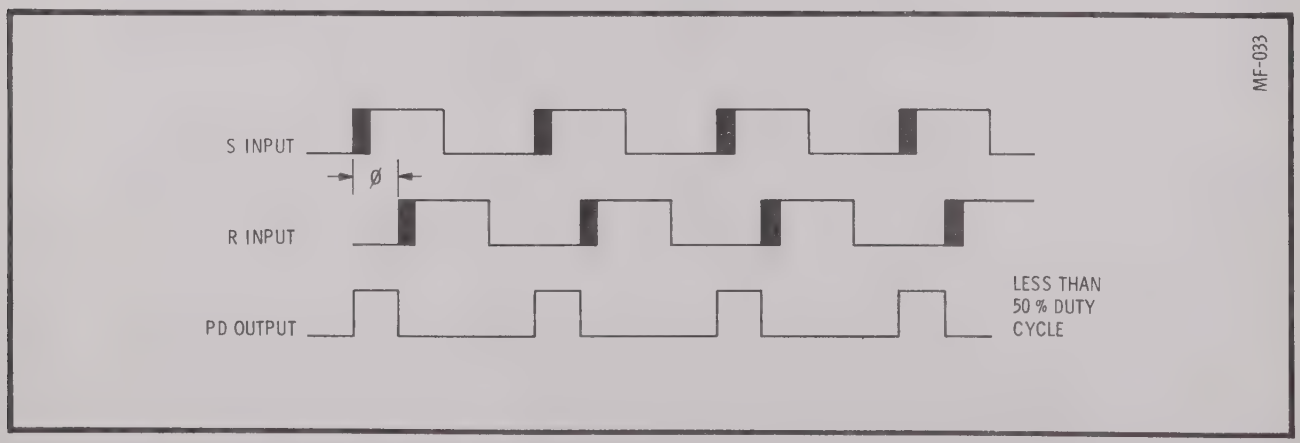


Figure 4-16. Phase Detector Output for $\phi < 180°$

‡The Model F52 does not provide the phase-lock feature.

and subharmonics can be tracked provided that the output frequency remains within the 10 Hz to 10 MHz limit.‡

The PHASE control shown in figure 4-14 performs two functions: when the fundamental is being tracked (that is, the voltage controlled generator signal frequency is the same as that of the input signal), this control varies the phase angle of the two signals by adding a d-c current through A1-R179 to the amplifier input terminal. This current forces the loop to stabilize at some phase angle that will cause the detector output to cancel the input current. The PHASE control is used to phase-lock a harmonic (or subharmonic) of the input frequency. The conditions for tracking the third harmonic of a signal are shown in figure 4-17. The phase detector output voltage has a net negative value. If a positive d-c voltage is added to the input signal via the PHASE control, the loop will be phase-locked to the input, but the function generator output signal will have a frequency of exactly three times the input frequency.‡

The description that follows covers the loop filter and its accessory circuits, as shown in the schematic diagram, figure 7-3.‡

The output waveform of the digital phase detector, swinging between zero and +2.4 volts, is first passed through a clamping circuit comprising transistor A1-Q31 and diodes A1-CR24 and A1-CR25. Resistors A1-R174 and A1-R175 offset the signal negatively using the -5 volt supply, and emitter follower A1-Q34 drives the clamping diodes through A1-R175. At diodes A1-TP34, the waveform is limited to ±0.6 volt peak swing. Changes in the input duty cycle (caused by phase errors at the phase detector input) appear at this point as a d-c level that can vary between the limits of the + and -0.6 volt. This d-c level is applied through A1-R180 to the inverting input of high gain amplifier A1-IC6. Depending on the range being used, the switch places one of six capacitors in the feedback path in series with damping resistor A1-R182. The noninverting input of the amplifier is returned to ground via A1-R183. Capacitors A1-C60 and A1-C62 and resistor A1-R176 are stabilizing components required by A1-IC6. At the output of amplifier A1-TP35, a voltage will exist which is the integral of the d-c phase level obtained at the diode clamp. Because of the presence of A1-R182 in the feedback path, this integral will have added to it a ripple

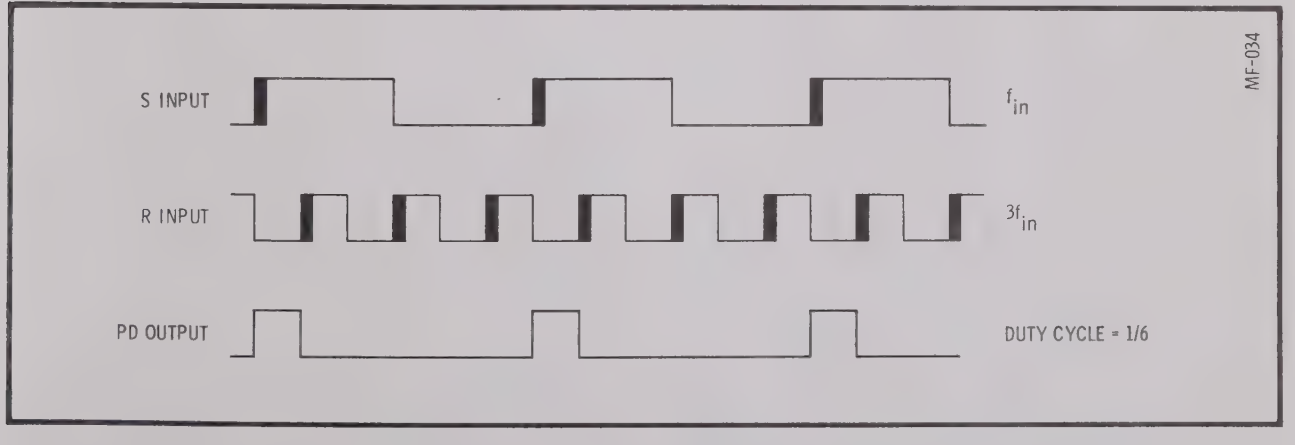


Figure 4-17. Third Harmonic Tracking

‡The Model F52 does not provide the phase-lock feature.

caused by the a-c signal of the clamped waveform.‡

In order to reduce this ripple to a minimum, a cancellation network is used, with a potentiometer A1-R189 as a summing point. Emitter-follower A1-Q32 applies the clamped waveform to a capacitor, also selected by the MULTIPLIER switch, and through A1-R188 to one end of A1-R189. The output of the integrating amplifier, through A1-R187, appears at the other end of A1-R189. As the a-c signals appear at the summing point in phase opposition, they cancel out and do not appear at the base of output emitter follower A1-Q33. The d-c level of the integrator output is not cancelled, and is used to drive A1-Q33, whose emitter output voltage is routed to the voltage controlled generator summing point. Transistor A1-Q34 works as a current source for A1-Q33.

4-13. POWER SUPPLY

Six regulated d-c power sources are required for the waveform generator circuits; these are ±5 volts, ±12 volts, and ±24 volts. These supplies are referenced to a single zener reference diode such that each voltage varies proportionally with the reference

The power supply (figure 7-7) consists of six fullwave rectifiers for use with the ±5 volt, ±12 volts, and ±24 volt regulators.

The raw dc is furnished by transformer A3-T1, rectifier diodes A3-CR1 through A3-CR4, A3-CR11 through A3-CR14, A3-CR27 through A3-CR30, and filter capacitors A3-C1, A3-C6, A3-C17, A3-C22, and A3-C27. When power is first applied, no +12 volts appears at A3-TP3 because amplifier A3-IC3, reference diode A3-CR20, and control transistor A3-Q7 have no power. Raw +5 volt and -5 volt power is furnished to A3-IC3 and A3-IC4 through diodes A3-CR23 and A3-CR22. Raw +12 volt power is supplied to A3-CR20 through A3-R25. Amplifier A3-IC3 thus senses a system unbalance, operates A3-Q9 which turns A3-Q7 on, and the +12 output begins to rise. This action continues until the current summation at A3-IC3 pin 4 is zero, whereupon the +12 volt output will hold at the voltage level set by A3-R28. Output filter capacitors A3-C14 and A3-C15 aid in reducing the impedance of the regulator. A3-Q8 is a current limit control. As more current is drawn through A3-Q7, an increasing voltage appears across A3-R20. When this voltage reaches approximately 0.7 volt, A3-Q8 turns on and clamps A3-Q7 base to A3-Q7 emitter. This clamp impedance is much lower than that of A3-R22 and ensures that the operation of A3-IC3 and A3-Q9 is negated.

The -12 volt regulator operates identically to the +12 volt system except that the operating level is determined by current summation of A3-R35 and A3-R36 at point A3-IC4 pin 4.

Plus and minus 24-volt regulating amplifiers A3-IC1 and A3-IC2 are referenced from the +12 volt output. The -24 volt supply voltage is determined by the +12 volt level by summing resistors A3-R16 and A3-R15. The +24 volt level is regulated by the -24 volt supply through resistors A3-R8 and A3-R9. Circuit operation of the 24 volt system is identical to that described for the +12 volt supply.

The plus and minus 5-volt regulating amplifiers A3-IC5 and A3-IC6 are referenced from the +12 volt output. The -5 volt supply voltage is determined by the +12 volt level by summing resistors A3-R53 and A3-R55 and adjusted by

‡The Model F52 does not provide the phase-lock feature.

potentiometer A3-R54. The +5 volt level is regulated by the -5 volt supply through resistors A3-R46 and A3-R47. Circuit operation of the 5-volt system is identical to that described for the +12 volt supply except for the raw power required by the integrated circuit.

Section V
CALIBRATION AND MAINTENANCE

5-1. INTRODUCTION

This section describes the procedures for proper maintenance and repair of the function generator. Included are performance checks, calibration and adjustment information, and a troubleshooting guide. Periodic maintenance is recommended; however, the overall stability and reliability of the instrument is such that, if used properly, it will provide years of uninterrupted service.

This section of the manual is divided into three basic areas: (1) performance verification, (2) calibration and adjustment, and (3) test point measurements and troubleshooting guide.

5-2. TEST EQUIPMENT REQUIRED

Table 5-1 lists the test equipment required to perform the procedures given in this section. The table includes the types of instruments required, their minimum specifications, and recommended models. If the recommended model is not available, any model which meets the minimum specifications may be substituted.

5-3. PERFORMANCE CHECKS

The following performance checks are designed to assist in comparing the function generator with its published specifications. These checks may be used for incoming inspection, periodic maintenance, and after-repair checks. The performance checks should be made before calibrating the instrument. If the instrument does not meet the requirements outlined in the performance checks, refer to the calibration procedure, paragraph 5-4, in this section.

Performance check data tables are provided throughout this section for recording the performance of the function generator during the performance checks. These tables may be duplicated and used to provide a permanent record if desired.

The performance check procedure consists of the following individual tests:

- Dial Accuracy Check
- Sinewave Frequency Response Check
- Sinewave Distortion Check
- Waveform Symmetry Check
- Squarewave and Pulse Overshoot and Rise-Time Check
- Offset Control Check
- Output Attenuator Check
- Variable Pulse Width Check
- VCB Input Check
- Trigger Sync Check
- Phase-Lock Check‡

‡The Model F52 does not provide the phase-lock feature.

TABLE 5-1. TEST EQUIPMENT REQUIRED

Type	Suggested Model	Minimun Specifications
Oscilloscope	Tektronix 585A	DC to 80 MHz
Oscilloscope Plug-In	Tektronix Type 1A5 with Type 81 Adapter	Differential Comparator 50 MHz
Oscilloscope Plug-In	Tektronix Type 82	Dual-Trace
Oscilloscope Probe	Tektronix Type P6008	X10 DC to 100 MHz
Oscilloscope Probe	Tektronix Type P6028	X1 DC to 33 MHz
Digital Voltmeter	Darcy 440	0.1 percent Accuracy, 0.1 mv resolution
Counter	Monsanto	5 Hz to 10 MHz, 5 Digits
Time Interval Counter	HP-5223L	0.1 percent Accuracy
DC Voltage Source	Conventional regulated bench supply	Variable - 10 mv
Distortion Analyzer	HP-331A	0.1 percent Full Scale 5 Hz to 600 kHz
Spectrum Analyzer	HP-8553L/8552L Display 140S	100 MHz 1 percent Accuracy
Pulse Generator	Electro Design PG-20	10 Hz to 10 MHz 5 ns Rise Time
Thermal Converter	HP-11049A	20 Hz to 10 MHz 0.1 percent Accuracy
BNC Attenuator	Tektronix 011-0069-01	2X Attenuator
50-ohm Termination	Tektronix 011-0049-01	50-ohm Feedthrough
Voltmeter (Hi-freq)	Boonton 91C	100 kHz to 20 MHz 1 percent Accuracy

a. DIAL ACCURACY CHECK.

Step 1. Connect the 50 OUTPUT terminal of the function generator to a counter through a 50-ohm feed-through terminal.

Step 2. Set the WAVEFORM switch at ⊓ .

Step 3. Set the OFFSET switch at ∿ .

Step 4. Press the CONT MODE pushbutton.

Step 5. Set the ATTENUATOR switch for 0 db.

Step 6. Set the frequency dial at the indicated values in table 5-2.

Step 7. Set the MULTIPLIER switch at the indicated values in table 5-2.

Step 8. The counter should read within the limits specified in table 5-2 for each indicated frequency.

Step 9. Set the WAVEFORM switch at ⋀ .

Step 10. The counter should read within the limits specified in table 5-3.

b. SINEWAVE FREQUENCY RESPONSE CHECK. - This procedure checks for signal amplitude variations within the tolerance limits. A thermal converter is used in this measurement because its operation is virtually independent of frequency. The percent of change of the thermal converter output should be about 1.7 times the percent of change of the input. Check the calibration report for the exact multiplier factor supplied with the thermal converter. Allow five seconds for the thermal converter to stabilize between readings.

Step 1. Set the OFFSET switch to ∿ .

Step 2. Press the CONT MODE pushbutton.

Step 3. Set the frequency to 10 kHz.

Step 4. Set the WAVEFORM switch to ⊓ .

Step 5. Using an oscilloscope, set the ATTENUATOR switch to 10 volts p-p on the 50 Ω OUTPUT with a 50-ohm load.

Step 6. Connect the equipment as shown in figure 5-1.

NOTE

The HP11049A thermal converter is rated for a maximum input of 3.0 vrms. Be careful not to exceed this input at any time.

Step 7. Measure the output voltage from the thermal converter.

Step 8. The maximum meter change converted from percent accuracy deviation is given by the following equation.

$$\text{Max. Meter Change} = \frac{\text{Percent Accuracy}}{100} \times \text{Multiplier Factor} \times \text{Meter Reading}$$

Example: Accuracy = 1%
Multiplier Factor = 1.7
Meter Reading = 10 mv

Maximum change allowed to be within

$$1\% = \frac{1}{100} \times 1.7 \times 10 \text{ ma} = 0.17 \text{ mv}$$

TABLE 5-2. DIAL ACCURACY VERIFICATION

Dial	Multiplier	Counter Reading	
		Low Limit	High Limit
0.5	0.001	1653 sec	2532 sec
5	0.001	194 sec	206 sec
10	0.001	98 sec	102 sec
0.5	0.01	165 sec	253 sec
5	0.01	19.4 sec	20.6 sec
10	0.01	9.8 sec	10.2 sec
0.5	0.1	16.5 sec	25.3 sec
5	0.1	1.94 sec	2.06 sec
10	0.1	0.98 sec	1.02 sec
0.5	1	1.65 sec	2.53 sec
5	1	0.194 sec	0.206 sec
10	1	0.098 sec	0.102 sec
0.5	10	165 m sec	253 m sec
5	10	19.4 m sec	20.6 m sec
10	10	9.8 m sec	10.2 m sec
0.5	100	39.5 Hz	60.5 Hz
5	100	485 Hz	515 Hz
10	100	980 Hz	1020 Hz
0.5	1 K	395 Hz	605 Hz
5	1 K	4.85 kHz	5.15 kHz
10	1 K	9.8 kHz	10.2 kHz
0.5	10 K	3.95 kHz	6.05 kHz
5	10 K	48.5 kHz	51.5 kHz
10	10 K	98 kHz	102 kHz
0.5	100 K	39.5 kHz	60.5 kHz
5	100 K	485 kHz	515 kHz
10	100 K	950 kHz	1050 kHz
0.5	1 M	285 kHz	715 kHz
5	1 M	4.65 MHz	5.35 MHz
10	1 M	9.2 MHz	10.8 MHz

TABLE 5-3. DIAL ACCURACY FOR RAMP AND PULSE WAVEFORMS

Dial	Multiplier	Counter Reading	
		Low Limit	High Limit
0.5	100 k	39.5 kHz	60.5 kHz
5	100 k	485 kHz	515 kHz
10	100 k	890 kHz	1110 kHz
0.5	1 M	350 kHz	650 kHz
5	1M	4.4 MHz	5.6 MHz

Step 9. To obtain the percent of variation from a change in the meter reading use the following equation.

$$\% \text{ Variation} = \frac{\text{Change in Meter Reading x 100}}{\text{Multiplier Factor x Meter Reading}}$$

Example: $\% = \frac{0.17 \text{ mv}}{1.7 \text{ x } 10 \text{ mv}} \text{ x } 100$

$\% = 1\%$

Step 10. Measure the amplitude change in the frequency ranges listed in table 5-4 and calculate the percent of variation.

c. SINEWAVE DISTORTION CHECK.

Step 1. Set the frequency dial to 10.

Step 2. Press the CONT MODE pushbutton.

Step 3. Set the MULTIPLIER switch to 1 K.

Step 4. Set the OFFSET switch to ⏦ .

Step 5. Set the WAVEFORM switch to ∿ .

Step 6. Connect the 50 Ω OUTPUT terminal to the distortion analyzer using a 50-ohm coaxial cable.

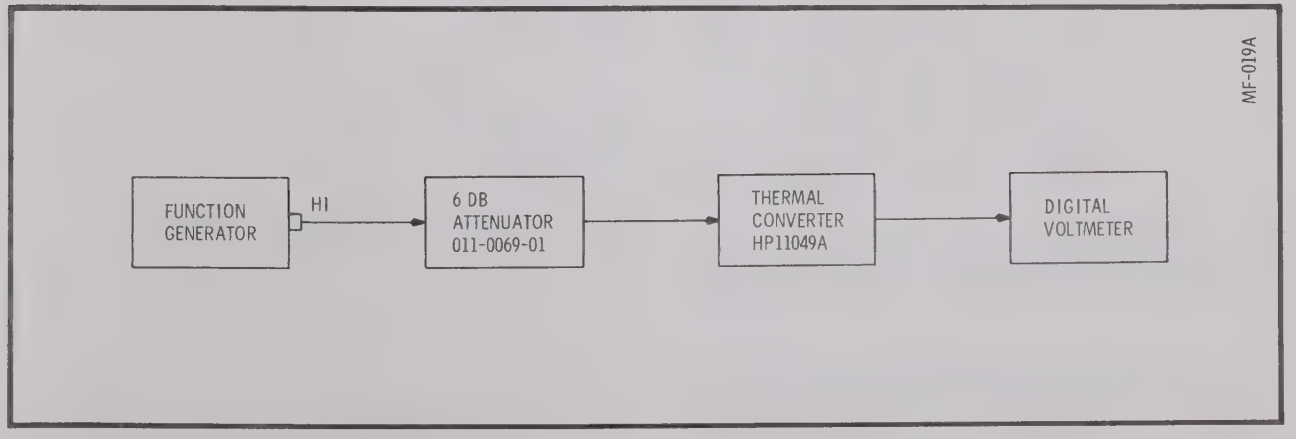


Figure 5-1. Frequency Response Test Setup

TABLE 5-4. FREQUENCY RESPONSE VARIATION

Frequency	Meter Reading	Percent Variation	Allowable Variation
0.0005 MHz to 100 kHz			±0.5 percent
100 kHz to 1 MHz			±1.0 percent
1 MHz to 5 MHz			±3.0 percent
5 MHz to 10 MHz			±5.0 percent

Step 7. Terminate the cable with the 50-ohm feed-through termination.

Step 8. Set the ATTENUATOR switch to 10 volts p-p using an oscilloscope on the 50 Ω OUTPUT.

Step 9. Set the analyzer controls to read the harmonic content of the 10-kHz signal. Harmonic distortion should be less than 0.5 percent.

Step 10. Make distortion measurements at the frequencies listed in table 5-5.

Step 11. The HP-331A distortion analyzer is useful only to 600 kHz; a spectrum analyzer should be used to check the harmonic content in the megahertz region.

NOTE

The HP-8553L spectrum analyzer input impedance is 50 ohms; therefore, the feed-through terminator should not be used with it. Also, be careful to keep the signal level into the instrument at less than 1 vrms.

d. WAVEFORM SYMMETRY CHECK.

Step 1. Set the frequency to a value in each frequency range specified in table 5-6.

Step 2. Press the CONT MODE pushbutton.

Step 3. Connect both inputs of the time interval to the function generator SYNC OUT terminal with a 50-ohm feed-through termination.

Step 4. Set channel A to +0.5 volt.

Step 5. Set channel B to -0.5 volt.

Step 6. Record time interval measurement in table 5-6.

Step 7. Set channel A to -0.5 volt.

Step 8. Set channel B to +0.5 volt.

Step 9. Record time interval measurement in table 5-6.

Step 10. The time measurements in steps 6 and 9 should be within the tolerance specified in table 5-6.

e. SQUAREWAVE, PULSE OVERSHOOT, AND RISE-TIME CHECK.

Step 1. Set the frequency to 1 MHz.

Step 2. Press the CONT MODE pushbutton.

Step 3. Set the OFFSET switch to ⏦ .

TABLE 5-5. SINEWAVE DISTORTION

Frequency	Measured Distortion	Allowable Distortion
0.0005 Hz to 100 kHz		<0.5 percent (-46 db)
100 kHz to 1 MHz		<1 percent (-40 db)
1 MHz to 5 MHz		<3 percent (-30 db)
5 MHz to 10 MHz		<5 percent (-25 db)

TABLE 5-6. WAVEFORM SYMMETRY

Frequency	Positve Slope	Negative Slope	Tolerance
0.0005 Hz to 10 Hz			<1.0 percent
10 Hz to 100 kHz			<0.5 percent
100 kHz to 3 MHz			<2.0 percent
3 MHz to 10 Hz			<5 percent

Step 4. Set the WAVEFORM switch to ⊓ .

Step 5. Connect a scope to the 50 Ω OUTPUT terminal by means of a 50-ohm coaxial cable and a 50-ohm feed-through terminator.

Step 6. Set the ATTENUATOR switch to 10 volts p-p.

Step 7. Observe the 10-volt p-p waveform for rise time and overshoot. Rise and fall times should not exceed 30 nsec.

Step 8. The overshoot should be less than 0.5 volt.

Step 9. Set the WAVEFORM switch to ⊓ and repeat step 7.

f. OFFSET CONTROL CHECK.

Step 1. Set the frequency to 1Kz.

Step 2. Set the WAVEFORM switch to ⊓ .

Step 3. Press the CONT MODE pushbutton.

Step 4. Set the OFFSET switch to ∿ .

Step 5. Connect the 50 Ω OUTPUT of the function generator to the oscilloscope. Use the 50-ohm termination at the oscilloscope input.

Step 6. Adjust the ATTENUATOR switch to obtain a scope display of 10 volts p-p; using the DC input setting.

Step 7. Turn the OFFSET switch to the ∿ position.

Step 8. The waveform should now appear at half amplitude, with its positive peaks at the zero voltage level.

Step 9. Rotate the OFFSET switch to the ∿ position and verify that the negative peaks of the waveform are at the zero voltage level.

g. OUTPUT ATTENUATOR CHECK.

Step 1. Set the frequency to 1 kHz.

Step 2. Set the WAVEFORM switch to ∿

Step 3. Set the OFFSET switch to ⏦

Step 4. Press the CONT MODE pushbutton.

Step 5. Connect a scope to the 50 Ω OUTPUT terminal with a type W plug-in.

Step 6. Set the OUTPUT ADJUST control to the CAL position.

Step 7. Connect a 50-ohm feed-through to the oscilloscope.

Step 8. Set the ATTENUATOR switch to the positions listed in table 5-7.

Step 9. The Vpp output voltage level should read within the limits specified in table 5-7.

TABLE 5-7. OUTPUT ATTENUATOR CALIBRATION

Position	50 Ω Output (into 50 Ω)	Tolerance
MAX	15 Vpp	None
0 db	10 Vpp	±2%
-10 db	3.16 Vpp	±2%
-20 db	1.0 Vpp	±2%
-30 db	0.316 Vpp	±2%
-40 db	0.1 Vpp	±2%
-50 db	0.0316 Vpp	±2%

h. VARIABLE WIDTH PULSE CHECK.

Step 1. Set the frequency dial to 10.0.

Step 2. Set the OFFSET switch to ⏦

Step 3. Set the WAVEFORM switch to VAR ⎍.

Step 4. Set the MULTIPLIER switch to 100.

Step 5. Press the CONT MODE pushbutton.

Step 6. Connect channel A of a dual trace oscilloscope to the 50 Ω OUTPUT terminal.

Step 7. Connect channel B to SYNC OUT.

Step 8. Rotate the VAR PULSE control between its extreme positions.

Step 9. Set the ATTENUATOR switch to MAX and the OUTPUT ADJUST control to the CAL position.

Step 10. Observe a waveform having a duty cycle which is variable from at least 5 percent to 95 percent of the 1-ms period of the waveform.

Step 11. Set the MULTIPLIER switch to 100K.

Step 12. Vary the setting of the VAR PULSE control and observe that the minimum pulse width is 100 ns or less, measured at half amplitude.

Step 13. Rotate the VAR PULSE control to the other end and observe that the minimum pulse width is 100 ns or less, measured at half amplitude.

Step 14. Set the MULTIPLIER switch to 1M.

Step 15. Set the frequency to 5.

Step 16. Connect an oscilloscope through a 50-ohm terminal and observe the variable pulse.

Step 17. The minimum voltage amplitude should be 12 volts p-p.

i. VCG INPUT CHECK.

Step 1. Set the frequency dial at its lower stop.

Step 2. Set the MULTIPLIER switch to 100.

Step 3. Connect a +10 volt variable source to the VCG INPUT.

Step 4. Connect a frequency counter to the SYNC OUT terminal.

Step 5. Connect a digital voltmeter to the VCG INPUT.

Step 6. A voltage of +10.0 ±0.7 volts should be applied for a frequency of 1.000 kHz.

j. TRIGGER SYNC CHECK.

Step 1. Connect a frequency counter to the SYNC OUT terminal of the function generator.

Step 2. Press the CONT MODE pushbutton.

Step 3. Set the function generator to 1000 ±2 Hz.

Step 4. Connect the counter to a pulse generator.

Step 5. Adjust the pulse generator amplitude to +10.0 volt.

Step 6. Set the pulse generator to 1010 ±2 Hz.

Step 7. Connect the + output of the pulse generator to the TRIGGER SYNC terminal.

Step 8. Set the OFFSET switch to ∿

Step 9. Prepare the oscilloscope with the dual trace plug-in.

Step 10. Connect channel A to the pulse generator.

Step 11. Connect channel B to the function generator 50 Ω OUTPUT terminal.

Step 12. Set the WAVEFORM switch to ⊓

Step 13. Adjust the ATTENUATOR switch for identical scope presentations.

Step 14. Externally trigger the scope from the pulse generator sync output terminal.

Step 15. Observe that the function generator output locks to the frequency of the pulse generator.

Step 16. Set the function generator to 1.000 MHz ±0.002 MHz.

Step 17. Set the pulse generator frequency to 1.010 MHz ±0.002 MHz.

Step 18. Set the pulse generator amplitude to +5 volts.

Step 19. Observe that the function generator locks to the pulse generator frequency.

Step 20. Press the TRIG MODE pushbutton.

Step 21. Set the pulse generator frequency to 100 kHz.

Step 22. Observe that pulse generator triggers the function generator output waveform.

k. PHASE-LOCK CHECK.‡

Step 1. Set the frequency dial to 5.

Step 2. Set the MULTIPLIER switch to 100.

Step 3. Set the PHASE CONTROL to the center of its rotation.

Step 4. Apply a 5-volt, p-p, 500 Hz, squarewave input signal to the TRIGGER SYNC terminal.

Step 5. Set the OFFSET switch to ∿

Step 6. Set the WAVEFORM switch to ⊓

Step 7. Press the ϕ LOCK pushbutton.

Step 8. Connect channel A of the dual trace oscilloscope to the input squarewave signal.

Step 9. Connect channel B of the oscilloscope to the 50 Ω OUTPUT terminal.

Step 10. Externally trigger the dual trace oscilloscope by using the SYNC OUT terminal.

Step 11. Verify that phase-lock has been achieved by simultaneously observing the waveforms of the two signal sources on the dual trace oscilloscope.

Step 12. If the two units are locked, the traces should appear stationary and at the same frequency, and the output signal should track the input frequency.‡

5-4. ADJUSTMENT AND CALIBRATION PROCEDURE

The following paragraphs contain a complete adjustment and calibration procedure for the function generator. This procedure should be performed only if it has been determined by the performance checks, paragraph 5-3, that the instrument is not operating within the published specifications. Voltage measurements are referenced to chassis ground. Adjustment locations are shown in figure 5-2 and test point locations in figure 5-3.

The detailed calibration procedures which are given below should be performed in the following order:

- Power Supply Calibration
- Dial Calibration
- Waveform Symmetry Calibration
- Triangle Amplitude Calibration
- Triangle Amplifier Gain Calibration
- Inverter DC Balance Calibration
- Compensated Level Control Calibration
- High Frequency Ramp Calibration
- Frequency Calibration
- Start/Stop Amplifier Calibration
- Sine Shaper Calibration
- Squarewave Amplitude Calibration
- Attenuator Calibration
- Output Summing Amplifier Calibration
- Output Amplifier Response Calibration
- Output Offset Calibration
- Phase-Lock Calibration‡

‡The Model F52 does not provide the phase-lock feature.

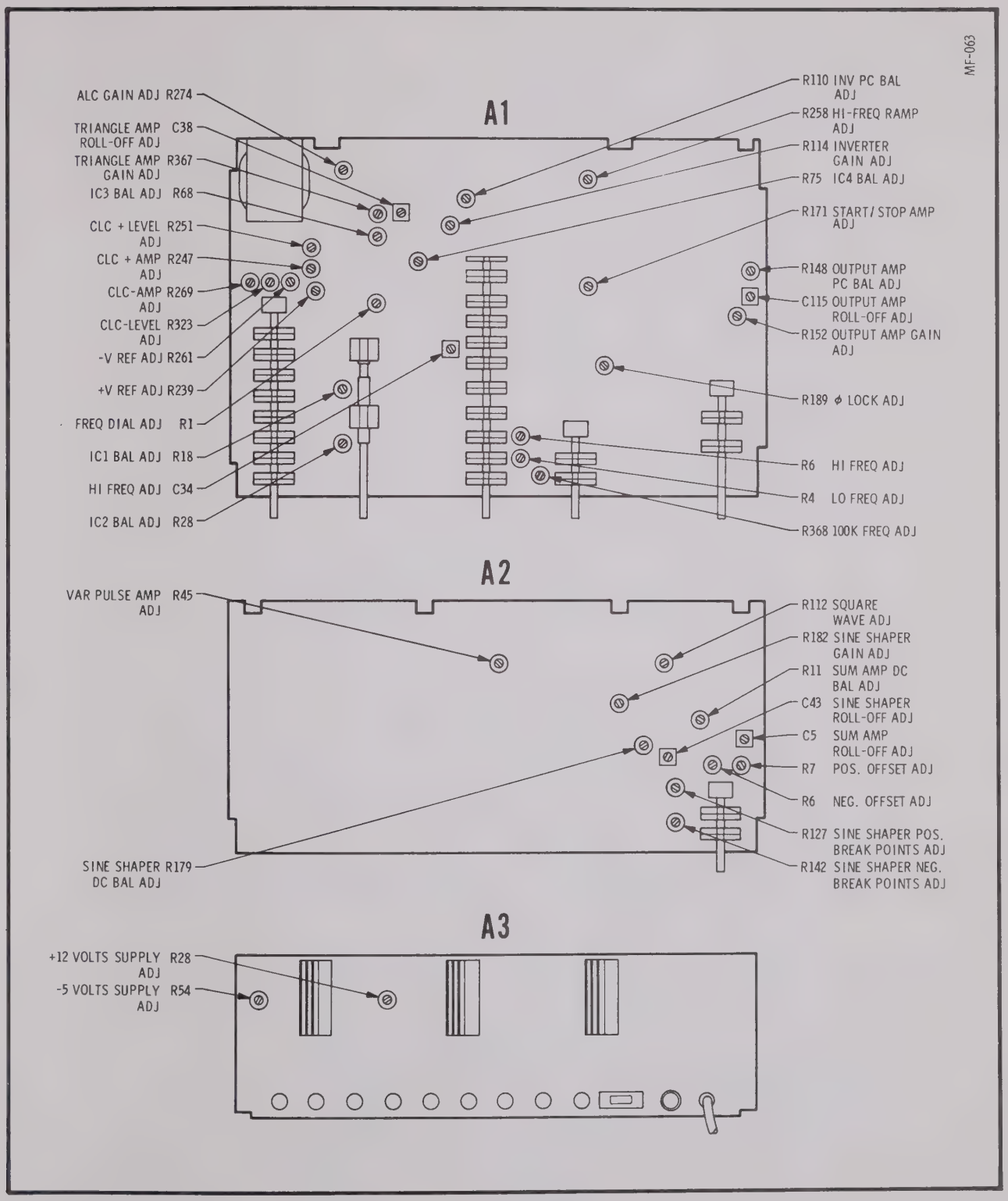

MF-063
A1
ALC GAIN ADJ R274
TRIANGLE AMP ROLL-OFF ADJ C38
TRIANGLE AMP GAIN ADJ R367
IC3 BAL ADJ R68
CLC + LEVEL ADJ R251
CLC + AMP ADJ R247
CLC-AMP ADJ R269
CLC-LEVEL ADJ R323
-V REF ADJ R261
+V REF ADJ R239
FREQ DIAL ADJ R1
IC1 BAL ADJ R18
HI FREQ ADJ C34
IC2 BAL ADJ R28
R110 INV PC BAL ADJ
R258 HI-FREQ RAMP ADJ
R114 INVERTER GAIN ADJ
R75 IC4 BAL ADJ
R171 START/STOP AMP ADJ
R148 OUTPUT AMP PC BAL ADJ
C115 OUTPUT AMP ROLL-OFF ADJ
R152 OUTPUT AMP GAIN ADJ
R189 ϕ LOCK ADJ
R6 HI FREQ ADJ
R4 LO FREQ ADJ
R368 100K FREQ ADJ
A2
VAR PULSE AMP ADJ R45
SINE SHAPER DC BAL ADJ R179
R112 SQUARE WAVE ADJ
R182 SINE SHAPER GAIN ADJ
R11 SUM AMP DC BAL ADJ
C43 SINE SHAPER ROLL-OFF ADJ
C5 SUM AMP ROLL-OFF ADJ
R7 POS. OFFSET ADJ
R6 NEG. OFFSET ADJ
R127 SINE SHAPER POS. BREAK POINTS ADJ
R142 SINE SHAPER NEG. BREAK POINTS ADJ
A3
+12 VOLTS SUPPLY ADJ R28
-5 VOLTS SUPPLY ADJ R54

Figure 5-2. Adjustment Locations

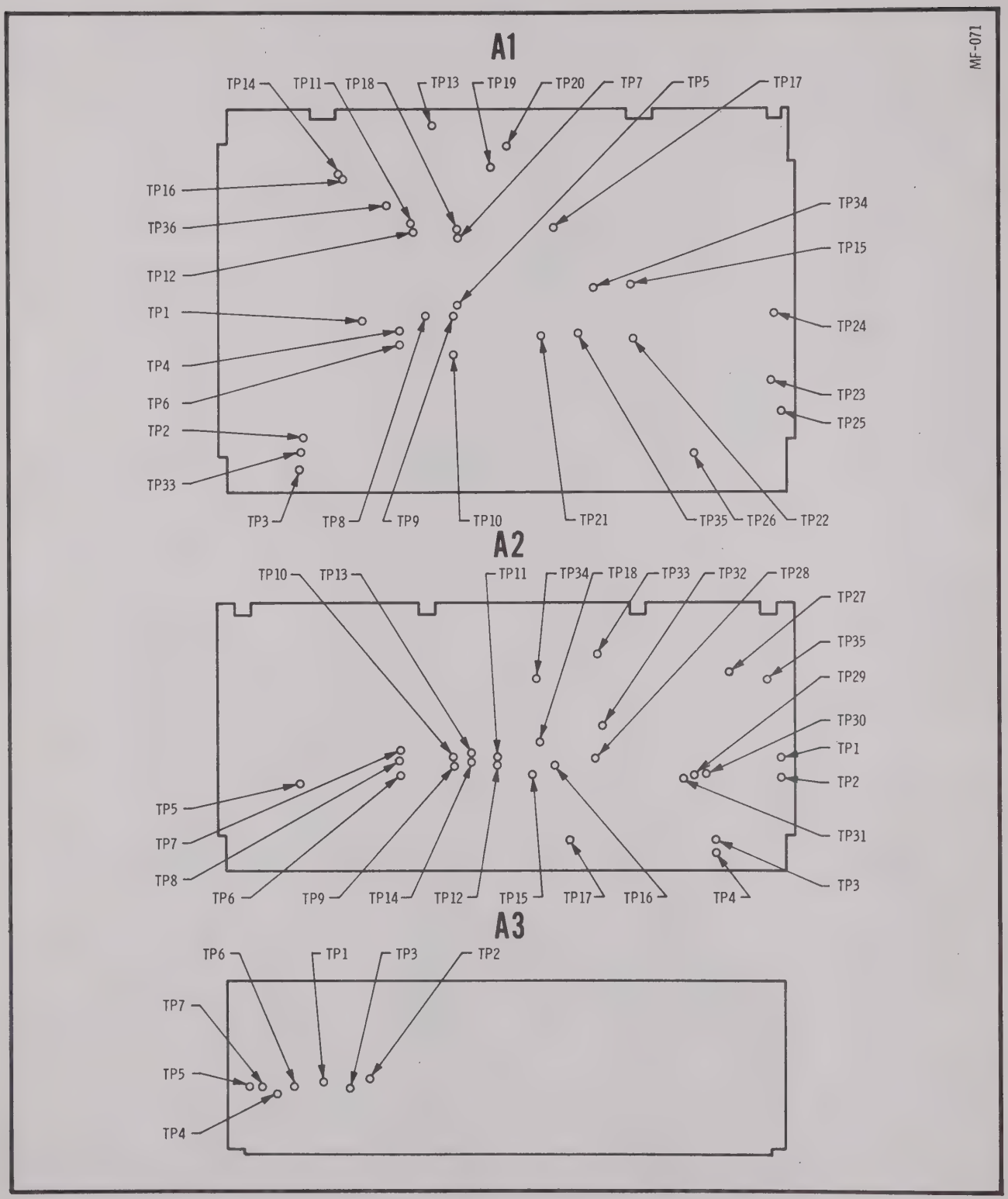


Figure 5-3. Test Point Locations

a. POWER SUPPLY CALIBRATION.

Step 1. Connect a digital voltmeter and oscilloscope to A3-TP3 and A3-TP4 (ground).

Step 2. Adjust potentiometer A3-R28 until the voltmeter indicates +12.00 volts ±5.0 mv.

Step 3. The ripple waveform should be less than 10 mv p-p.

Step 4. Connect a digital voltmeter to A3-TP7 and A3-TP4 (ground).

Step 5. Adjust A3-R54 for a voltmeter reading of -5.00 ±0.01 volts.

Step 6. Using the voltmeter and oscilloscope, measure the voltages at the test points listed in table 5-8.

Step 7. If any of the voltage measurements are out of tolerance, correct the trouble before continuing with the calibration procedure.

b. DIAL CALIBRATION.

Step 1. Set the potentiometer A1-R1 to the midrange position.

Step 2. Set the frequency dial fully clockwise until cursor indicator lines up with the 1 portion of the 0.1 dial mark.

Step 3. Connect the digital voltmeter between A1-TP1 and A1-TP33 (ground).

Step 4. Loosen the hex nut on potentiometer A1-R3 and hold A1-R3 while performing the next step.

Step 5. Turn the frequency dial slowly clockwise while observint that the voltmeter indicates a voltage decreasing linearly to less than 120 mv. (The body of A1-R3 may require rotating to obtain less than 120 mv).

Step 6. With the frequency dial set at 0.1, adjust the body of potentiometer A1-R3 until the voltmeter indicates 145 ±5 mv.

Step 7. Holding the body of potentiometer A1-R3 (of step 6), secure the hex nut and again measure the voltage at A1-TP1.

Step 8. If step 7 is out of the acceptance limits, repeat steps 1 through 7.

c. WAVEFORM SYMMETRY CALIBRATION.

Step 1. Connect the digital voltmeter between A1-TP5 and A1-TP3.

Step 2. Adjust potentiometer A1-R18 until the voltmeter indicates +0.050 volt ±5 mv.

Step 3. Set the MULTIPLIER switch to 100.

Step 4. Set the frequency dial to 5.

Step 5. Connect a floating digital voltmeter between A1-TP8 and A1-TP3.

Step 6. Record the voltmeter reading.

Step 7. Reconnect the voltmeter between A1-TP6 and A1-TP2.

Step 8. Adjust potentiometer A1-R28 to obtain a voltmeter indication equal to the previous reading within ±2 mv.

TABLE 5-8. POWER SUPPLY VOLTAGES

Test Point	Expected Voltage	Tolerance	Maximum Ripple (Millivolts)
A3-TP3	+12.00 vdc	±10 mv	10
A3-TP7	-12.00 vdc	±60 mv	10
A2-TP1	+24.00 vdc	±120 mv	20
A3-TP4	-24.00 vdc	±150 mv	20
A3-TP2	+ 5.00 vdc	±200 mv	5
A3-TP3	- 5.00 vdc	±10 mv	5

Step 9. Connect a floating digital voltmeter between A1-TP4 and A1-TP6.

Step 10. Adjust potentiometer A1-R68 until an indication of 0.000 volt ±1 mv is obtained.

Step 11. Disconnect the voltmeter of step 9 and reconnect it between A1-TP5 and A1-TP8.

Step 12. Adjust potentiometer A1-R75 until an indication of 0.000 volt ±1 mv is obtained.

d. TRIANGLE AMPLITUDE CALIBRATION.

Step 1. Set the MULTIPLIER switch to 100.

Step 2. Set the frequency dial to 10.

Step 3. Set potentiometer A1-R274 to its midrange position.

Step 4. Set the WAVEFORM switch to ∿ .

Step 5. Connect a digital voltmeter to A1-TP18 and A1-TP34 (ground).

Step 6. Adjust potentiometer A1-R239 to obtain a voltmeter indication of +2.700 ±0.005 volts.

Step 7. Connect the digital voltmeter to A1-TP19 and A1-TP34 (ground).

Step 8. Adjust potentiometer A1-R261 to obtain a voltmeter indication of -2.700 to ±0.005 volts.

Step 9. Set the MULTIPLIER switch to 1M.

Step 10. Set the frequency dial to 3.

Step 11. Connect an oscilloscope with a 1A5 plug-in unit to A1-TP14.

Step 12. Adjust A1-R274 until the triangle waveform negative peak is -3.000 ±0.010 volts.

e. TRIANGLE AMPLIFIER GAIN CALIBRATION.

Step 1. Set the frequency dial to 10.

Step 2. Set the MULTIPLIER switch to 100.

Step 3. Connect an oscilloscope with 1A5 plug-in to A1-TP11 and A1-TP9 (ground) and record the amplitude of the triangle.

Step 4. Connect an oscilloscope to A1-TP14.

Step 5. Adjust A1-R367 to obtain four times the amplitude obtained in step 3, within ±1 percent.

f. INVERTER DC BALANCE CALIBRATION.

Step 1. Set the WAVEFORM switch to ⎍ .

Step 2. Connect the digital voltmeter between A1-TP13 and A1-TP9 (ground).

Step 3. Adjust potentiometer A1-R110 until the voltmeter indicates 0.00 ±0.01 volt.

g. COMPENSATED LEVEL CONTROL CALIBRATION.

Step 1. Set the frequency dial to the midrange position (5.0).

Step 2. Set the MULTIPLIER switch to 1M.

Step 3. Connect a signal generator with a 10 Vpp sinewave at 100 kHz to the VCG INPUT terminal.

Step 4. Connect an oscilloscope to A1-TP14.

Step 5. Adjust A1-R247 for approximately the same positive peak amplitude of all triangle waves.

Step 6. Adjust A1-R269 for approximately the same negative peak amplitude of all triangle waves.

Step 7. Adjust A1-R251 for a positive average peak triangle amplitude of +3.0 volts.

Step 8. Adjust A1-R323 for a negative average peak triangle amplitude of -3.0 volts.

h. HIGH FREQUENCY RAMP CALIBRATION.

Step 1. Set the OFFSET switch to ⏦ .

Step 2. Set WAVEFORM switch to ⋀ .

Step 3. Set the frequency to 3.0 MHz.

Step 4. Connect an oscilloscope to A1-TP14.

Step 5. Adjust A1-R258 for minimum aberrations.

i. FREQUENCY CALIBRATION.

Step 1. Set the WAVEFORM switch to ∿ .

Step 2. Connect a counter to SYNC OUT terminal and press the CONT MODE pushbutton.

Step 3. Set the frequency dial to 10.

Step 4. Set the MULTIPLIER switch to 100.

Step 5. Set the OFFSET switch to ⏦ .

Step 6. Adjust A1-R1 for a frequency of 1000 +1 Hz.

Step 7. Recheck at frequency dial setting of 0.5, observing a frequency reading of 50 ±5 Hz.

Step 8. Rotate the frequency dial clockwise to its lower stop.

Step 9. Record the frequency indicated on the counter (< 10 Hz.)

Step 10. If steps 7 and 9 are not within the tolerance, repeat dial calibration procedure.

Step 11. Set the frequency dial to 8.

Step 12. Set the MULTIPLIER switch to 0.1.

Step 13. Adjust A1-R4 for a period of 1.250 ±0.005 seconds.

Step 14. Set the MULTIPLIER switch to 1K.

Step 15. Adjust A1-R6 for a frequency of 8035 ±5 Hz.

Step 16. Set the MULTIPLIER switch to 10K.

Step 17. Verify that the frequency is 80 kHz ±400 Hz.

Step 18. If step 17 is not satisfactory, readjust potentiometer A1-R6 and repeat steps 14 through 17.

Step 19. Set the MULTIPLIER switch to 1M.

Step 20. Set the frequency dial to 8.

Step 21. Adjust trimmer A1-C34 for an 8.0 MHz indication on the counter.

Step 22. Set the frequency dial to 10.0.

Step 23. Set the MULTIPLIER switch to 1M.

Step 24. Adjust trimmer capacitor A1-C38 for a frequency of 10.0 ±0.03 MHz.

Step 25. Set the frequency to 2.0 MHz.

Step 26. Adjust A1-T274 for a frequency of 2 MHz ±100 kHz.

Step 27. Repeat steps 14 through 26 until dial settings are within tolerance.

Step 28. Set the MULTIPLIER switch to 100K.

Step 29. Adjust A1-R368 for a frequency of 800 ±4 kHz.

j. START/STOP AMPLIFIER CALIBRATION.

Step 1. Set the frequency dial at 10.

Step 2. Set the MULTIPLIER switch to 1K.

Step 3. Set the PHASE and TRIGGER LEVEL controls to the center of their rotation.

Step 4. Press the TRIG MODE pushbutton.

Step 5. Connect an oscilloscope at A1-TP14.

Step 6. Set the SWEEP/SEC switch to 1K and the VERNIER to the CAL position.

Step 7. If the triggered waveform does not appear, readjust the TRIGGER LEVEL control.

Step 8. Adjust A1-R171 for 0 vdc centerline during the waveform off time.

k. SINE SHAPER CALIBRATION.

Step 1. Set the frequency to 50 kHz.

Step 2. Set the WAVEFORM switch to ∿ .

Step 3. Set the OFFSET switch to ∿ .

Step 4. Connect a short jumper lead between A2-TP29 and A2-TP3 (ground).

Step 5. Connect a short jumper lead from A1-TP11 to A1-TP9 (ground).

Step 6. Connect the digital voltmeter between A2-TP32 and ground.

Step 7. Adjust A2-R179 for 0 volts ±10 mv at A2-TP32.

Step 8. Remove jumper leads on A2-TP29 and A1-TP11.

Step 9. Connect an oscilloscope to the SINE MON terminal.

Step 10. Press the CONT MODE pushbutton.

Step 11. Connect a distortion analyzer or spectrum analyzer to the SINE MON terminal. (NOTE: the HP-8553 spectrum analyzer input impedance is 50 ohms.)

Step 12. Alternately adjust A2-R127 and A2-R142 for minimum total distortion.

Step 13. If the distortion analyzer is used, total harmonic distortion should be less than 0.5 percent.

Step 14. If the spectrum analyzer is used, all harmonics should be -50 db below the fundamental frequency.

Step 15. Connect a type 585A oscilloscope with a type 1A5 plug-in to A2-TP32.

Step 16. Adjust A2-R182 for a positive wave amplitude of +3.0 ±0.015 volts.

Step 17. Connect a high frequency voltmeter to A2-TP32.

Step 18. Set the MULTIPLIER switch to 1M.

Step 19. Rotate the frequency dial from 5 to 10 and adjust A2-C43 for a maximum flat response of 2.08 ±0.06 vrms or a voltmeter deviation reading of ±3 percent.

l. SQUAREWAVE AMPLITUDE CALIBRATION.

Step 1. Set the frequency to 1 kHz.

Step 2. Press the CONT MODE pushbutton.

Step 3. Set the WAVEFORM switch to ⊓ .

Step 4. Connect a type 585A oscilloscope with type 1A5 plug-in to A2-TP27.

Step 5. Adjust A2-R112 for a positive waveform level of +3.0 ±0.015 volts.

m. ATTENUATOR CALIBRATION.

Step 1. Set the frequency to 1 kHz.

Step 2. Set the OFFSET switch to ∿ .

Step 3. Press the CONT MODE pushbutton.

Step 4. Set the WAVEFORM switch to ∿ .

Step 5. Connect a 585A oscilloscope with a 50-ohm load and type 1A5 plug-in to the 50 Ω OUTPUT terminal.

Step 6. Rotate the OUTPUT ADJUST control to the CAL position.

Step 7. Set the ATTENUATOR switch to 10 Vpp.

Step 8. Adjust A1-R152 for a positive peak waveform level of +5 ±0.025 volts.

n. OUTPUT SUMMING AMPLIFIER CALIBRATION.

Step 1. Set the OFFSET switch to ∿ .

Step 2. Set the frequency dial to 10.0.

Step 3. Set the MULTIPLIER switch to 1K.

Step 4. Set the WAVEFORM switch to ∿ .

Step 5. Connect a short jumper between A2-TP2 and A2-TP3 (ground).

Step 6. Connect the digital voltmeter to A2-TP35 and A2-TP3 (ground).

Step 7. Adjust A2-R11 until the voltmeter reads less than ±0.005 volt.

Step 8. Set the ATTENUATOR switch to the 0-db position.

Step 9. Connect a short jumper between A1-TP23 and A1-TP25 (ground).

Step 10. Connect the voltmeter to the 50 Ω OUTPUT terminal.

Step 11. Adjust A1-R148 until the voltmeter reads less than ±0.02 volt.

Step 12. Remove the jumpers installed at A2-TP2 and A1-TP23.

o. OUTPUT AMPLIFIER RESPONSE CALIBRATION.

Step 1. Set the WAVEFORM switch to ∿ .

Step 2. Press the CONT MODE pushbutton.

Step 3. Set the MULTIPLIER switch to 1 M.

Step 4. Set the frequency dial to 1.0.

Step 5. Set the OFFSET switch to ⏦ .

Step 6. Set the ATTENUATOR switch to 0 db and the OUTPUT ADJUST control to the CAL position.

Step 7. Connect a high frequency voltmeter to A2-TP35 and the probe ground to A2-TP3.

Step 8. Measure and record the voltmeter reading.

Step 9. Rotate the frequency dial from 1.0 to 10.0 and adjust A2-C5 for a maximum flat response of the voltmeter reading obtained in step 8 (within a tolerance of 0 to -3 percent).

Step 10. Connect a high frequency voltmeter to the 50 Ω OUTPUT by means of a 50-ohm coaxial cable. Use the 50-ohm feed-through termination adapter at the voltmeter end of the cable.

Step 11. Set the frequency dial to 1.0.

Step 12. Measure and record the voltmeter reading.

Step 13. Rotate the frequency dial from 1.0 to 10.0 and adjust A1-C115 for a maximum flat response for the voltmeter reading obtained in step 12 (within a tolerance of +0 to -5 percent).

p. OUTPUT OFFSET CALIBRATION.

Step 1. Set the frequency to 100 Hz.

Step 2. Set the WAVEFORM switch to ⎍ .

Step 3. Set the OFFSET switch to ⏦ .

Step 4. Press the CONT MODE pushbutton.

Step 5. Connect the 50 Ω OUTPUT of the function generator to the oscilloscope. Use the 50-ohm termination at the oscilloscope input.

Step 6. Adjust the ATTENUATOR switch to obtain an oscilloscope display of 10 volts p-p, using the d-c input setting.

Step 7. Set the OFFSET switch to ⏦ .

Step 8. The waveform should now appear at half amplitude, with its positive peaks at the zero voltage level ±50 mv.

Step 9. Adjust A2-R6 to obtain this condition.

Step 10. Rotate the OFFSET switch to the position and verify that the negative peaks of the waveform are at zero volts ±50 mv.

Step 11. Adjust A2-R7 to obtain this condition.

Step 12. Set the OFFSET switch to ADJ.

Step 13. Rotate the OFFSET ADJUST control fully counter-clockwise. No part of the waveform should cross the zero level in the positive direction.

Step 14. Rotate the OFFSET ADJUST control fully clockwise. No part of the waveform should cross the zero level in the negative direction.

q. PHASE LOCK CALIBRATION.‡

Step 1. Set the frequency dial to 5.

Step 2. Set the MULTIPLIER switch to 100.

Step 3. Set the PHASE control to the center of its rotation.

Step 4. Apply 5-Vpp, 500-Hz, squarewave input signal to the TRIGGER SYNC terminal.

Step 5. Set the OFFSET switch to .

Step 6. Set the WAVEFORM switch to .

Step 7. Press the ϕ LOCK pushbutton.

Step 8. Connect channel A of a dual trace oscilloscope to the input squarewave signal.

Step 9. Connect channel B to the 50 Ω OUTPUT terminal.

Step 10. Externally trigger the oscilloscope, using the SYNC OUT terminal.

Step 11. Verify that phase lock has been achieved by simultaneously observing the waveforms of the two signal sources on the dual trace oscilloscope.

Step 12. If the two units are locked, the traces should appear stationary, and at the same frequency.

Step 13. Connect the oscilloscope to A1-TP22.

Step 14. Adjust A1-R189 for a minimum peak-to-peak voltage amplitude of the waveform.‡

5-5. TROUBLESHOOTING

The following paragraphs cover most of the individual circuits and are intended to help in the quick repair of the function generator. Refer to the functional block diagram, figure 7-1, and circuit schematics, figure 7-3, 7-5, and 7-7. An illustrative table containing all of the testpoint measurements is also included. The following topics are covered in this section.

- Power Supply
- Voltage Level Sensor and Automatic Level Control
- Triangle Amplifier
- Inverter Amplifier
- Frequency Control and Voltage-to-Current Converter
- Variable Pulse Width Shaper
- Test-Point Measurements

‡The Model F52 does not provide the phase-lock feature.

a. POWER SUPPLY TROUBLESHOOTING. - When the power supply is turned on, d-c voltages are established in sequence. The +12 volt supply starts first and provides a reference for the -12 volt supply. When the -12 volt output is established, a power source for the -5 volt regulator is provided. Presence of +12 volts powers the 24-volt regulator amplifiers, and the -24 volt supply will start, followed by the +24 volt supply. Thus, if +12 volt power is not present, no other voltages can be present. If -12 volt is missing, +24, -24, and -5 will be missing. If -24 volts is not operating, +24 will not operate. The only voltages which do not affect the operation of other voltage regulators are +5 and +24 volts.

In the case of incorrect voltages, the sequence to be followed is +12, -12, +5, -5, -24, and +24. If one or more voltages are incorrect, proceed as follows:

Step 1. Check the pilot lamp for presence of line power and fuse.

Step 2. Check for presence of d-c voltages according to the sequence listed.

Step 3. Check for a possible short or overcurrent on the affected supply. A3-Q2, A3-Q5, A3-Q8, A3-Q11, A3-Q14, A3-Q17 provide current limiting which reduces the 5, 12 and 24-volt lines to zero when overloads are present.

Step 4. If low voltages are present in the 5, 12, or 24-volt systems and no overload currents are present:

(1) Check overload transistors A3-Q2, A3-Q5, A3-Q8, A3-Q11, A3-Q14, and A3-Q17 for leakage or shorts.

(2) Check collector leads of A3-Q3, A3-Q4, A3-Q9, A3-Q10, A3-Q15, and A3-Q16. These collectors approach ground potential when an increase in output voltage is sensed by the regulator amplifiers A3-IC1 through A3-IC6.

(3) Check pass transistors A3-Q1, A3-Q6, A3-Q7, A3-Q12, A3-Q13, and A3-Q18 for open collectors. This condition is evident if the base of the pass transistor is 0.6 volt closer to ground than its emitter.

Step 5. If high voltages are present in the 12 or 24-volt systems, check pass transistors A3-Q1, A3-Q6, A3-Q7, A3-Q12, A3-Q13, and A3-Q18 for shorts.

b. VOLTAGE LEVEL SENSOR AND AUTOMATIC LEVEL CONTROL TROUBLESHOOTING. - The most likely cause of abnormal operation is within the VLS, because of its critical speed requirements. Obvious component failure should always be investigated initially, which might typically lead to one of the following:

(1) Improper reference voltages V_R (+) or V_R(-).

(2) Improper clamp voltage +3 or -3 volts.

(3) Incorrect d-c condition in ALC.

(4) Incorrect currents delivered to tunnel diodes.

(5) Failure of the latch circuit to toggle.

If no obvious component failures can be found, waveforms at A1-TP17 and A1-TP20 give the best clues as to causes of improper

operation. A1-TP17, at a d-c level of +12 volts, should exhibit a nominal 1-volt negative pulse at the positive triangle peak, and a nominal 3-volt positive pulse at the negative triangle peak.

The waveform at A1-TP20 is approximately +12.5 volts during the positive going ramp, and at approximately +11.7 volts during the negative going ramp. At the negative peak, a short duration pulse of +11.3 volts is normally present. (Refer to test point waveforms, table 5-10).

NOTE

If A1-R171 is not properly adjusted, the function generator will not operate; therefore, this control should be checked carefully.

c. TRIANGLE AMPLIFIER TROUBLESHOOTING. - In the event of major difficulty within the triangle amplifier, it is probable that the main integrator will also be inoperative. In this event, ground A1-TP10, then check for correct d-c conditions within the amplifier circuit. Because of the straightforward circuitry, a stage-by-stage d-c check should give adequate clues.

d. INVERTER AMPLIFIER TROUBLESHOOTING. - Similar procedures can be followed for inverter amplifier troubleshooting, because of the similarities of design. In the case of the inverter, a main loop signal may be available to assist, in the event that the triangle amplifier is still operative. If this is the case, simply set the WAVEFORM switch to either a positive-going ramp (◿) or a pulse(⎍) to obtain the test signal.

e. FREQUENCY CONTROL AND VOLTAGE-TO-CURRENT CONVERTER TROUBLESHOOTING. - Because the prime function of the frequency control and voltage-to-current converter is to generate known currents, the first item to check should be current level. This is best accomplished by connecting a low impedance milliameter (or microameter) between A1-TP10 and ground. This action will stall the integrator loop and make d-c measurements possible. The polarity of this current should be the same as the polarity of the voltage present at A1-TP7. Table 5-9 lists the maximum current generated on each range, for 50/50 duty cycle functions. (Frequency dial at 10.)

(1) Following a determination of incorrect current levels, and whether or not they are a function of A1-TP7 polarity, there should now be some clues as to the source of the problem. Note that in order to obtain a desired polarity at A1-TP7, it may be necessary to force the

TABLE 5-9. INTEGRATOR CURRENT AT 50/50 DUTY CYCLE VERSUS FREQUENCY MULTIPLIER SETTING

Multiplier	Maximum Current
0.001	300 na
0.01	3 μa
0.1	30 μa
1	3 μa
10	30 μa
100	300 μa
1 K	30 μa
10 K	300 μa
100 K	1.5 ma
1 M	7.5 ma

voltage level sensor circuitry into the desired state. This can be accomplished by momentarily clipping a grounded 470-ohm resistor to either A1-TP17 or A1-TP20.

(a) If proper current levels exist for negative polarity, the problem can be isolated to the area of A1-IC3, A1-IC2, A1-S1-5, and A1-S1-3.

(b) If neither polarity at A1-TP7 causes the proper current flow, this points to possible problems with A1-IC1 circuitry.

(2) In the event of less obvious problems, such as poor waveforms at low frequencies, one should suspect excessive leakage current at the integrator. Low frequency operation requires total leakage in the nanoamp region, and any of several components should be suspected, as should be the possibility of grease, dirt, or moisture on the circuit board itself.

f. VARIABLE PULSE WIDTH SHAPER TROUBLESHOOTING. - Verify the presence of a 6-volt p-p triangular waveform at the input to A2-R27. Provided the waveform does exist, a nominal 0 to +4 volt pulse should then be present at A2-TP33. The presence of this pulse verifies the operation of comparator A2-IC1. Further signal tracing through the discrete driver circuits A2-Q10 to A2-Q13 should lead to the source of difficulty.

g. TEST POINT WAVEFORMS. - Table 5-10 lists the d-c voltages or signal waveforms at each test point. The test point conditions are as follows unless specified otherwise:

INITIAL CONDITIONS

(1) PWR pushbutton	- Depressed
(2) CONT MODE pushbutton	- Depressed
(3) Frequency dial	- 10
(4) MULTIPLIER switch	- 100
(5) Frequency	- 1.0 kHz
(6) WAVEFORM switch	- ⎍
(7) OFFSET switch	- ⎓
(8) ATTENUATOR switch	- MAX
(9) OUTPUT ADJUST	- CAL

All measurements are made with respect to ground.

TABLE 5-10. TEST POINT MEASUREMENTS

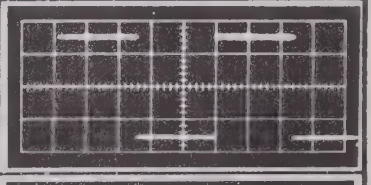
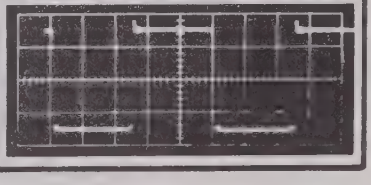
Test Point	Conditions	Comments	Measurement
A1-TP1 (Freq Control)	Note (1)	Read dc	+10 volts
A1-TP2 (V_A)	Note (1)	Read dc	+17.5 volts
A1-TP3 (V_B)	Note (1)	Read dc	-17.5 volts
A1-TP4 (V_C)	Note (1)	Read dc	+7.5 volts
A1-TP5 (V_D)	Note (1)	Read dc	-7.5 volts
A1-TP6 (Positive Current Source)	Note (1)	Read dc	+7.5 volts
A1-TP7 (VLS Output)	Note (1)	H = 0.2 ms/cm V = 2 v/cm + 0.7 Volt level	
	Note (2)	H = 0.2 μs/cm V = 2 v/cm + 0.7 Volt level	

Table 5-10. Test Point Measurements (Continued)

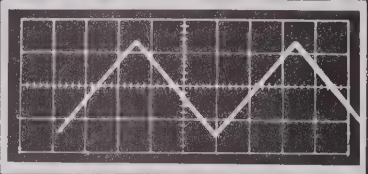
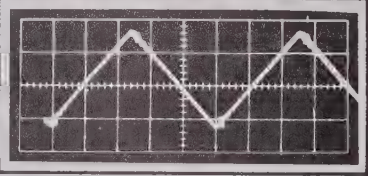
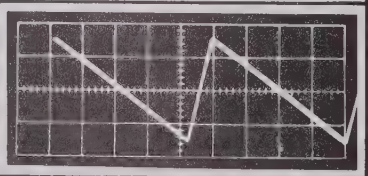
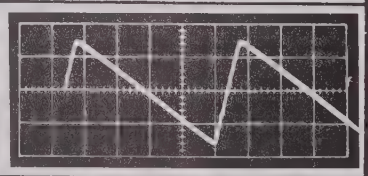
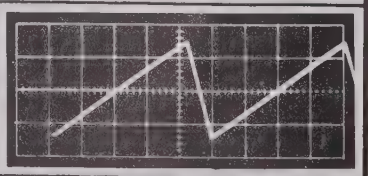
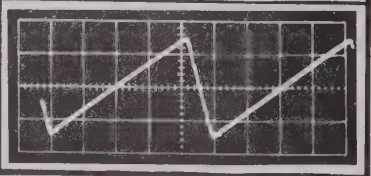
Test Point	Conditions	Comments	Measurement
A1-TP8 (Negative Current Source)	Note (1)	Read dc	-7.5 volts
A1-TP9 (GND)			0 volts
A1-TP10 (Triangle Generator)	Note (1)	H = 0.2 ms/cm V = 0.5 v/cm	
	Note (2)	H = 0.2 μs/cm V = 0.5 v/cm	
A1-TP11	Same as TP 10		
A1-TP12 (Inverter Input)	Note (1) WAVEFORM ✓	H = 0.2 ms/cm V = 2 v/cm	
	Note (2) WAVEFORM ✓	H = 0.2 μs/cm V = 2 v/cm	
A1-TP13 (Inverter Output)	Note (1) WAVEFORM ✓	H = 0.2 ms/cm V = 2 v/cm	
	Note (2) WAVEFORM ✓	H = 0.2 μs/cm V = 2 v/cm	

Table 5-10. Test Point Measurements (Continued)

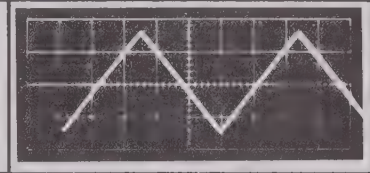
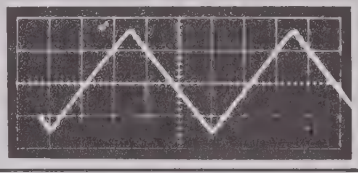
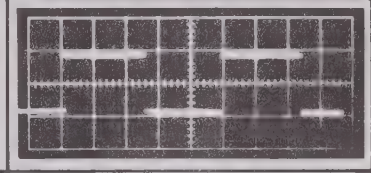
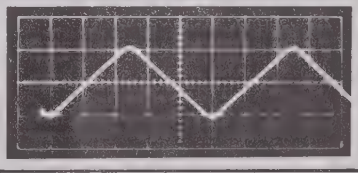
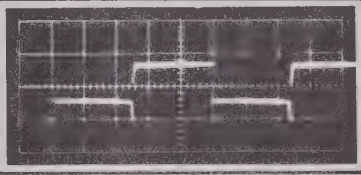
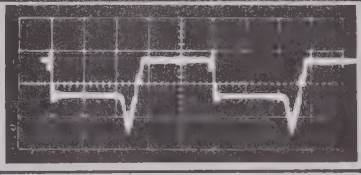
Test Point	Conditions	Comments	Measurement
A1-TP14 (Triangle Amplifier Output)	Note (1)	H = 0.2 ms/cm V = 2 v/cm	
	Note (2)	H = 0.2 ms/cm V = 2 v/cm	
A1-TP15 (ϕ LOCK Input)	Notes (1) and (3) Press ϕ LOCK	H = 0.2 ms/cm V = 2 v/cm	
A1-TP16 (ALC Input)	Note (2)	H = 0.2 μs V = 2 v/cm	
A1-TP17 (Tunnel Diode Triggering)	Note (1)	H = 0.2 ms/cm V = 0.5 v/cm +12 Volt level	
	Note (2)	H = 0.2 μs/cm V = 0.5 v/cm +12 Volt level	
A1-TP18 ($+V_{Ref}$)	Note (1)	Read dc	+3 volts
	Note (2)	Read dc	+2 volts
	Note (1) MULTIPLIER IM (1 MHz)	Read dc	0 volts

Table 5-10. Test Point Measurements (Continued)

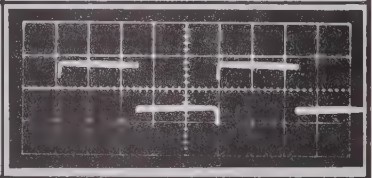
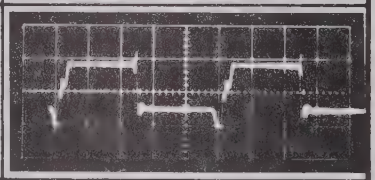
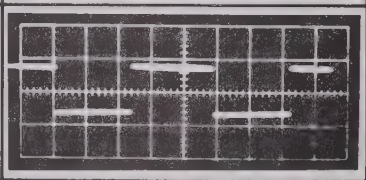
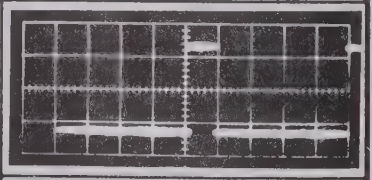
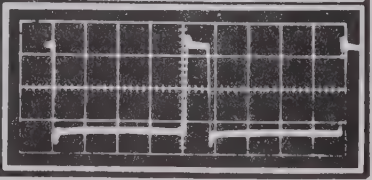
Test Point	Conditions	Comments	Measurement
A1-TP19 ($-V_{Ref}$)	Note (1)	Read dc	-3 volts
	Note (2)	Read dc	-2 volts
	Note (1) MULTIPLIER IM (1 MHz)	Read dc	0 volts
A1-TP20 (Tunnel Diode Triggering)	Note (1)	H = 0.2 ms/cm V = 0.5 v/cm +12 Volt level	
	Note (2)	H = 0.2 μs/cm V = 0.5 v/cm +12 Volt level	
A1-TP21 (ϕ LOCK Filter Output)	Notes (1) and (3) Press ϕLOCK	H = 0.2 ms/cm V = 1 v/cm	
A1-TP22 (ϕ LOCK Output)	Note (1) and (3) Press ϕ LOCK	Read dc	< ± 1.0 volt
A1-TP23 (Output Amplifier Input)	Note (1) WAVEFORM ⎍	H = 0.2 ms/cm V = 2 v/cm	
	Note (2) WAVEFORM ⎍	H = 0.2 μs/cm V = 2 v/cm	

Table 5-10. Test Point Measurements (Continued)

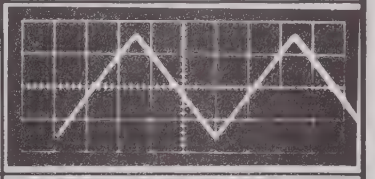
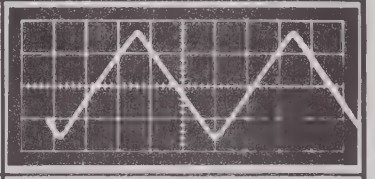
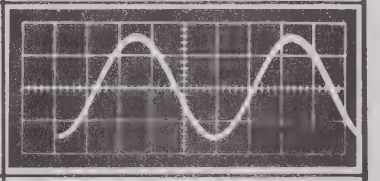
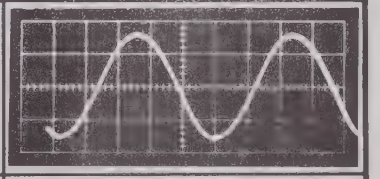
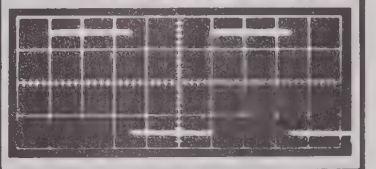
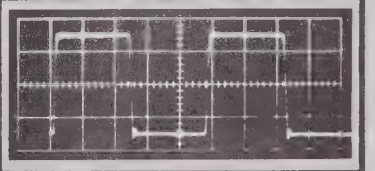
Test Point	Conditions	Comments	Measurement
A1-TP24 (Output Amplifier Output)	Note (1)	H = 0.2 ms/cm V = 10 v/cm	
	Note (2)	H = 0.2 μs/cm V = 10 v/cm	
	Note (1) WAVEFORM ∿	H = 0.2 ms/cm V = 10 v/cm	
	Note (2) WAVEFORM ∿	H = 0.2 μs/cm V = 10 v/cm	
	Note (1) WAVEFORM ⊓	H = 0.2 ms/cm V = 10 v/cm	
	Note (2) WAVEFORM ⊓	H = 0.2 μs/cm V = 10 v/cm	
A1-TP25 (GND)			0 volts
A1-TP26 (GND)			0 volts

Table 5-10. Test Point Measurements (Continued)

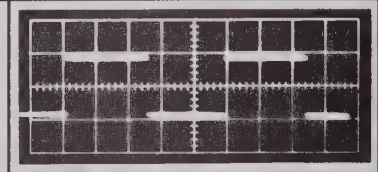
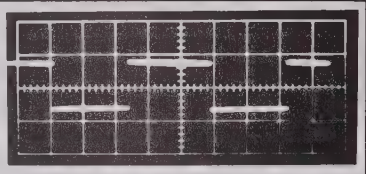
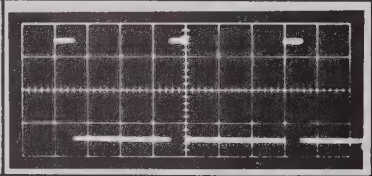
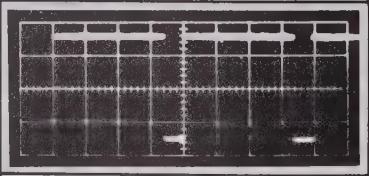
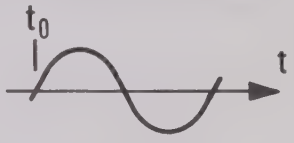
Test Point	Conditions	Comments	Measurement
A1-TP33 (GND)			0 volts
A1-TP34 (Phase-Lock Filter Input)	Notes (1) and (3) Press ϕ LOCK	H = 0.2 ms/cm V = 0.5 v/cm	
A1-TP35 (Phase-Lock Filter Output)	Notes (1) and (3) Press ϕ LOCK	H = 0.2 ms/cm V = 0.1 v/cm	
A1-TP36 (GRD)			0 volts
A2-TP1 (Output Summing Amplifier Input)	Note (1) WAVEFORM ⌐⌐	H = 0.2 ms/cm V = 2 v/cm	
A2-TP2 (Output Summing Amplifier Input)	Note (1) WAVEFORM _⌐	H = 0.2 ms/cm V = 1 v/cm	
A2-TP3 (GND)			0 volts
A2-TP4 (Offset Adjust)	Note (1) Set to ADJ (Max CW)	Read dc	-12 volts

Table 5-10. Test Point Measurements (Continued)

TRIGGER LOGIC SEQUENTIAL TIMING DIAGRAM			
Test Point	Conditions	Comments	Measurement
TRIGGER SYNC Input (BNC)	Notes (1) and (3) TRIGGER LEVEL Centered Press TRIG SLOPE		
A2-TP5	Note (3) Press GATE or BURST	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	

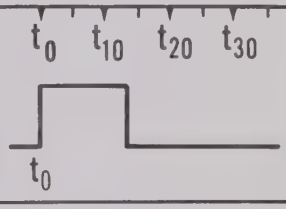
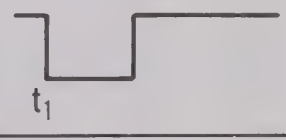
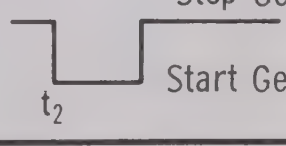
GATE OR BURST MODE SEQUENCE			
Test Point	Conditions	Comments	Measurement
A2-TP7	Note (3) Press GATE or BURST	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	
A2-TP8	Note (3) Press GATE or BURST	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	
A2-TP9	Note (3) Press GATE or BURST	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volts	

Table 5-10. Test Point Measurements (Continued)

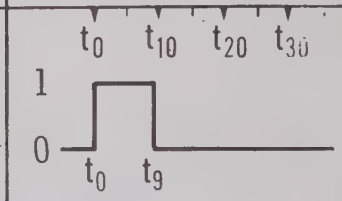
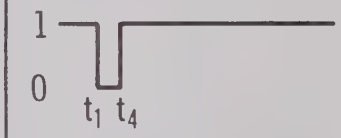
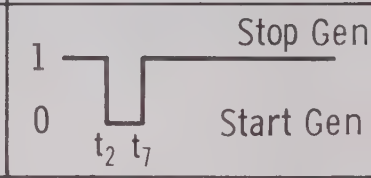
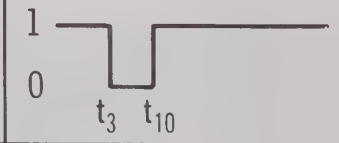
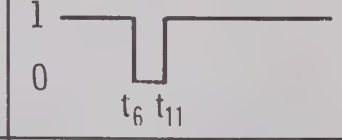
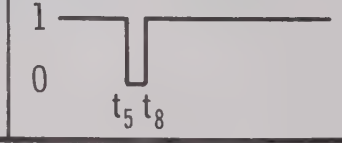
TRIGGER MODE SEQUENCE			
Test Point	Conditions	Comments	Measurement
A2-TP7	Note (3) Press TRIG MODE	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	
A2-TP8	Note (3) Press TRIG MODE	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	
A2-TP9	Note (3) Press TRIG MODE	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	
A2-TP6	Note (3) Press TRIG MODE	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	
A2-TP13	Note (3) Press TRIG MODE	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	
A2-TP10	Note (3) Press TRIG MODE	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	

Table 5-10. Test Point Measurements (Continued)

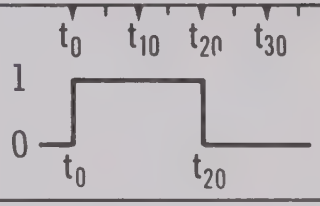
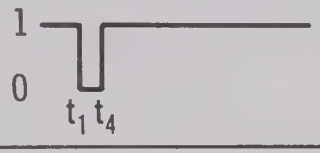
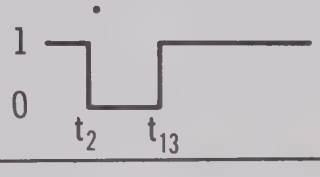
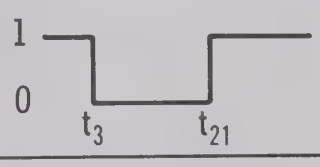
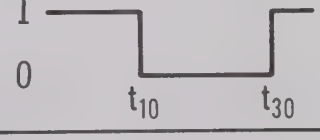
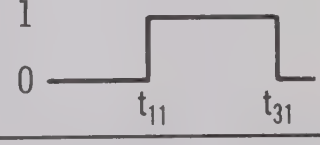
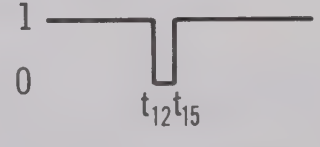
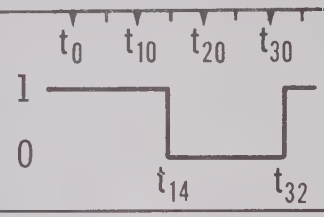
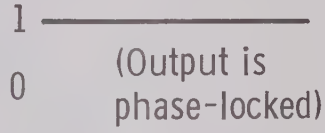
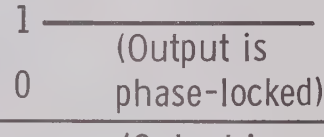
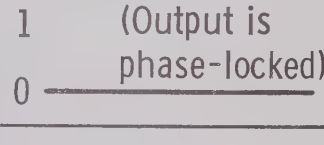
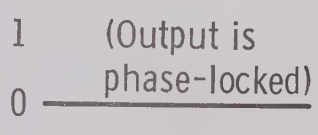
PHASE LOCK SEQUENCE			
Test Point	Conditons	Comments	Measurement
A2-TP7	Note (3) Press ϕLOCK	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	
A2-TP8	Note (3) Press ϕLOCK	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	
A2-TP9	Note (3) Press ϕLOCK	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	
A2-TP6	Note (3) Press ϕLOCK	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	
A2-TP13	Note (3) Press ϕLOCK	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	
A2-TP11	Note (3) Press ϕLOCK	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	
A2-TP14	Note (3) Press ϕLOCK	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	

Table 5-10. Test Point Measurements (Continued)

Phase Lock Sequence (continued)			
Test Point	Conditions	Comments	Measurement
A2-TP12	Note (3) Press ϕ LOCK	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	
A2-TP15	Note (3) Press ϕ LOCK	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	
A2-TP16	Note (3) Press ϕ LOCK	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	
A2-TP17	Note (3) Press ϕ LOCK	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	
A2-TP18	Note (3) Press ϕ LOCK	Logic 1 ≥ 3 volts Logic 0 ≤ 0.7 volt	

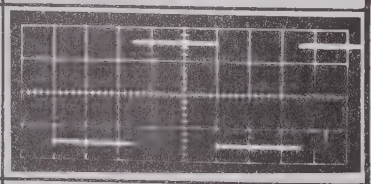
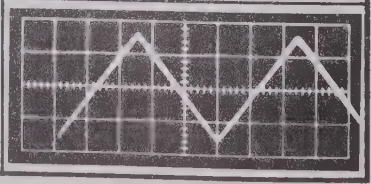
Test Point	Conditions	Comments	Measurement
A2-TP27 (Squarewave Output)	Note (1)	H = 0.2 ms/cm V = 2 v/cm	
A2-TP28 (Triangle Input)	Note (1)	H = 0.2 ms/cm V = 2 v/cm	

Table 5-10. Test Point Measurements (Continued)

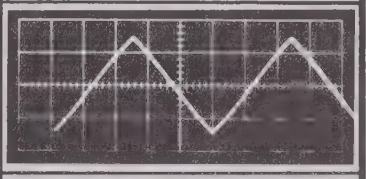
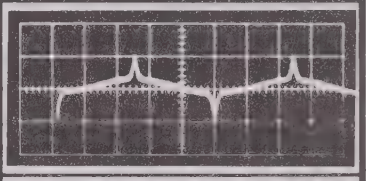
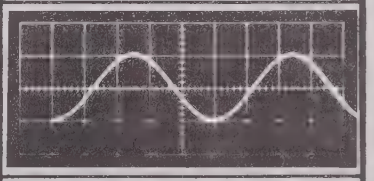
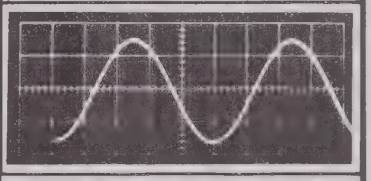
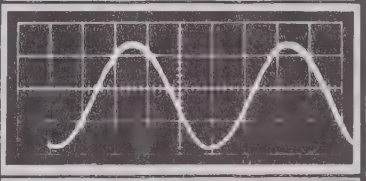
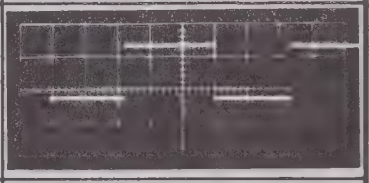
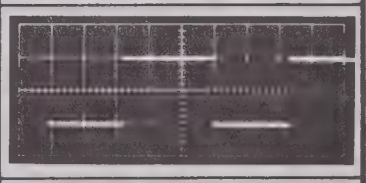
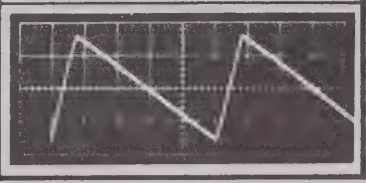
Test Point	Conditions	Comments	Measurement
A2-TP29 (Sine Shaper Input)	Note (1)	H = 0.2 ms/cm V = 2 v/cm	
A2-TP30 (Sine Shaper)	Note (1)	H = 0.2 ms/cm V = 0.5 v/cm	
A2-TP31 (Sine Shaping)	Note (1)	H = 0.2 ms/cm V = 2 v/cm	
A2-TP32 (Sine Shaper Output)	Note (1)	H = 0.2 ms/cm V = 2 v/cm	
A2-TP32 (Sine Shaper Output)	Note (2)	H = 0.2 μs/cm V = 2 v/cm	
A2-TP33 (Comparator Output)	Note (1) WAVEFORM ⎍ VAR PULSE control at center	H = 0.2 ms/cm V = 2 v/cm	
A2-TP34 (Pulse Width Output)	Note (1) WAVEFORM ⎍ VAR PULSE control at center	H = 0.2 ms/cm V = 5 v/cm	
A2-TP35 (Output Summing Amplifier Output)	Note (1) WAVEFORM ⟋	H = 0.2 ms/cm V = 2 v/cm	

Table 5-10. Test Point Measurements (Continued)

Test Point	Conditions	Comments	Measurement
A3-TP1 (+24 Volt Supply		Read dc	+24 volts
A3-TP2 (-24 Volt Supply)		Read dc	-24 volts
A3-TP3 (+12 Volt Supply)		Read dc	+12 volts
A3-TP4 (GND)			0 volts
A3-TP5 (-12 Volt Supply)		Read dc	-12 volts
A3-TP6 (+5 Volt Supply)		Read dc	+5 volts
A3-TP7 (-5 Volt Supply)		Read dc	-5 volts

NOTES:

(1) See conditions specified in paragraph 5-5g

(2) See conditions specified in paragraph 5-5g except set MULTIPLIER = 100K
Frequency = 1 MHz

(3) In addition to specified conditions in paragraph 5-5g, connect a 5 Vpp, 1 KHz sine wave at the TRIGGER SYNC terminal and set the PHASE and TRIGGER LEVEL controls at center of rotation

Section VI
REPLACEABLE PARTS

6-1. INTRODUCTION

This section contains information for identifying and ordering replacement parts. Replacement parts may be ordered from Interstate Electronics Corporation. Be certain that the order or inquiry identifies the part by description and part number.

Table 6-1 is a listing of all manufacturers supplying parts used in the function generator. Manufacturers are listed in numerical order by their respective code symbols.

6-2. PARTS LIST TABLES

Tables 6-2 through 6-5 list all electrical and electronic parts in alphanumeric order by reference designators and provide the following information for each part, where applicable: (a) value, (b) description, (c) total quantity used in the instrument listed the first time the part number appears), (d) IEC part number, (e) manufacturer's code symbol, and (f) original manufacturer's part number. Mechanical parts are listed at the end of each table.

TABLE 6-1. LIST OF MANUFACTURERS

Code	Manufacturer
00287	CEM Co. Inc., Danielson, Connecticut
00779	AMP Inc., Harrisburg, Pennsylvania
00853	Sangamo Electric Co., S. Carolina Division, Pickens, South Carolina
01121	Allen-Bradley Co., Milwaukee, Wisconsin
01295	Texas Instruments Inc., Semiconductor-Components Division, Dallas, Texas
02114	Ferroxcube Corp., Of America, Saugerties, New York
02615	Nylok Corp., Paramus, New Jersey
02650	Amphenol Connector Division, Chicago, Illinois
02735	RCA Solid State and Receiving Tube Division, Somerville, New Jersey
03508	GE Co., Semi-Conductor Products Dept., Syracuse, New York
03877	Transitron Electronic Corporation, Wakefield, Massachusetts
03879	Akron Controller and Motor Inc., Akron, Ohio
04552	Emerson and Cuming Inc., Canton, Massachusetts
04713	Motorola Semiconductor Products Inc., Pheonix, Arizona
05820	Wakefield Engineering Inc., Wakefield, Massachusetts

Table 6-1. List of Manufacturers (Continued)

Code	Manufacturer
06540	Amaton Electronic Hardware Co. Inc., New Rochelle, New York
06915	Richco Plastic Co., Chicago, Illinois
07263	Fairchild Camera and Inst. Corp., Mountain View, California
07421	Interstate Electronics Corp., Anaheim, California
07933	Raytheon Co., Lexington, Massachusetts
12324	Stake Fastener Co., South El Monte, California
13740	Kanarr Corp., Kingston, Pennsylvania
28480	Hewlett-Packard Co., Palo Alto, California
28520	Heyman Mfg. Co., Kenilworth, New Jersey
49956	Raytheon Co., Lexington, Massachusetts
56289	Sprague Electric Co., North Adams, Massachusetts
56878	Standard Pressed Steel, Unbrako Division, Jerkintown, Pennsylvania
70903	Belden Mfg. Co., Chicago, Illinois
71450	CTS Corp., Elkhart, Indiana
71785	Cinch Mfg. Co. and Howard B. Jones Div., Chicago, Illinois
72136	Electric Motive Mfg. Co. Inc., Willimantic, Connecticut
74970	E. F. Johnson Co., Waseca, Minnesota
75042	I R C Inc., Phildelphia, Pennsylvania
75915	Littelfuse Inc., Des Plaines, Illinois
76381	Minnesota Mining and Manufacturing Co., St. Paul, Minnesota
76493	J. W. Miller Co., Los Angeles, California
77969	Rubbercraft Corp. of Calif. Ltd., Torrance, California
78189	Shakeproof Division of Illinois Tool Works, Elgin, Illinois
80294	Bourns Inc., Riverside, California
82389	Switchcraft, Inc., Chicago, Illinois
83330	Herman H. Smith Inc., Brooklyn, New York
84171	ARCO Electronics Inc., Great Neck, New York
84411	TRW Capacitor Division, Ogallala, Negraska
86928	Seastrom Mfg. Co. Inc., Glendale, California
90201	Mallory Capacitor Co., Indianapolis, Indiana
93332	Sylvania Electric Products Inc., Semiconductor Division, Woburn, Massachusetts
95987	Weckesser Co., Chicago, Illinois
97979	Reon Resistor Corp., Yonkers, New York
98978	International Electronic Research Corp., Burbank, California
61637	Union Carbide Corporation, New York, New York

TABLE 6-2. TOP ASSEMBLY PARTS LIST

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
		Function Generator, Model F53	1	P00334000-2		
		Function Generator, Model F53 (for Rack Mount)	1	P00334000-6		
		Function Generator, Model F52	1	P00334000-1		
		Function Generator, Model F52 (for Rack Mount)	1	P00334000-5		
A1		Main Board Assembly, F53	1	P00334100-2		
A1		Main Board Assembly, F52	1	P00334100-1		
A2		Auxiliary Board Assembly, F53	1	P00334200-2		
A2		Auxiliary Board Assembly, F52	1	P00334200-1		
A3		Power Supply Board Assembly	1	P00334300-1		
		Power Supply Board Assembly (for Rack Mount)	1	P00334300-2		
		Package Assembly	1	P00332000-2		
		Package Assembly (for Rack Mount)	1	P00332000-4		
		Front Panel, F53	1	P00334042		
		Front Panel, F52	1	P00334043		
		Rear Panel	1	P00334046		
		Knob Assembly, Frequency	1	P00333146		
		Knob, Frequency Vernier	1	P00333024-9		
		Knobs, Wave Form and Var Pulse	1	P00333024-2		
		Knob, Multiplier	1	P00333024-6		
		Knobs, Attenuator and Output Adjust	1	P00333024-5		
		Knobs, Phase and Trigger Level	1	P00333024-7		
		Knobs, Offset and Adjust	1	P00333024-1		
		Switch, Mode, F53	1	P00334034		
		Switch, Mode, F52	1	P00334036		
		Switch, Power	1	P00334031		
		Cursor	1	P00333041		
		Stand Off, Hinged	3	P00333321		
		Name Plate	1	468-003-005		
		Screw, Thread Cutting, Pan Head, Phillips Recessed	7			
		Jumper, Nickel Plated	1			
		Harness Wrap, Natural, 6"	1			
		Decal	1	P00334038		
		Screw, Flat Head, 6-32 x 3/8 LG	2			
		Screw, Pan Head, 6-32 x 3/8 LG	2			
		Screw, Pan Head, Cross Recessed	4			

TABLE 6-3. MAIN BOARD (A1) PARTS LIST

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
A1		P.C. Board Assy, Main Generator	Ref	P00334100-4		
R1	250Ω	R: Variable 1/4 Watt ±20%	2			
R2	10Ω	R: Metal Glaze 1/2 Watt ±5%	1			
R3	1K	Potentiometer, Freq	1			
R4	2.5K	R: Variable 1/4 Watt ±20%	3			
R5	1K	R: Metal Film 1/4 Watt ±1%	1			
R6	2.5K	R: Variable 1/4 Watt ±20%				
R7	11.3K	R: Metal Film 1/4 Watt ±1%	1			
R8	4.75K	R: Metal Film 1/4 Watt ±1%	1			
R9	12.4K	R: Metal Film 1/4 Watt ±1%	1			
R10	20K	R: Metal Film 1/4 Watt ±1%	1			
R11	12.4K	R: Metal Film 1/4 Watt ±1%	1			
R12	1.8K	R: Metal Glaze 1/2 Watt ±5%	2			
R13	910Ω	R: Metal Glaze 1/4 Watt ±5%	4			
R14	4.7K	R: Metal Glaze 1/4 Watt ±5%	5			
R15	750Ω	R: Metal Glaze 1/4 Watt ±5%	6			
R16	330K	R: Metal Glaze 1/4 Watt ±5%	1			
R17	1.5K	R: Metal Glaze 1/4 Watt ±5%	9			
R18	50K	R: Variable 1/4 Watt ±20%	5			
R19-R20	12.1K	R: Metal Film 1/4 Watt ±0.1%	2			
R21	1.8K	R: Metal Glaze 1/2 Watt ±5%				
R22	750Ω	R: Metal Glaze 1/4 Watt ±5%				
R23	1.5K	R: Metal Glaze 1/4 Watt ±5%				
R24	910Ω	R: Metal Glaze 1/4 Watt ±5%				
R25	1K	R: Metal Film 1/4 Watt ±1%	4			
R26	2.05K	R: Metal Film 1/4 Watt ±1%	2			
R27	10K	R: Metal Film 1/4 Watt ±1%	2			
R28	500Ω	R: Variable 1/4 Watt ±20%	5			
R29	10K	R: Metal Film 1/4 Watt ±1%				
R30	1K	R: Metal Film 1/4 Watt ±1%				
R31	2.05K	R: Metal Film 1/4 Watt ±1%				
R32-R35	1M	R: Metal Film 1/2 Watt ±0.25%	10			
R36	332K	R: Metal Film 1/4 Watt ±0.25%	2			
R37	115K	R: Metal Film 1/4 Watt ±0.25%	3			
R38	33.2K	R: Metal Film 1/4 Watt ±0.25%	2			
R39	6.65K	R: Metal Film 1/4 Watt ±0.25%	2			
R40	1.33K	R: Metal Film 1/4 Watt ±0.25%	2			
R41-R44	1M	R: Metal Film 1/2 Watt ±0.25%				
R45	332K	R: Metal Film 1/4 Watt ±0.25%				
R46	115K	R: Metal Film 1/4 Watt ±0.25%				

EL F52/F53 , Main Board (A1) Parts List (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
R47	33.2K	R: Metal Film 1/4 Watt ±0.25%				
R48	6.65K	R: Metal Film 1/4 Watt ±0.25%				
R49	1.33K	R: Metal Film 1/4 Watt ±0.25%				
R50	115K	R: Metal Film 1/4 Watt ±0.25%				
R51	76.8K	R: Metal Film 1/4 Watt ±0.25%	1			
R52	10Ω	R: Metal Glaze 1/4 Watt ±5%	6			
R53	665K	R: Metal Film 1/2 Watt ±0.25%	1			
R54	210K	R: Metal Film 1/4 Watt ±0.25%	1			
R55	23.2K	R: Metal Film 1/4 Watt ±0.25%	1			
R56	4.64K	R: Metal Film 1/4 Watt ±0.25%	1			
R57	931Ω	R: Metal Film 1/4 Watt ±0.25%	1			
R58	1M	R: Metal Film 1/2 Watt ±0.25%				
R59	121K	R: Metal Film 1/4 Watt ±0.25%	1			
R60	1M	R: Metal Film 1/2 Watt ±0.25%				
R61	432K	R: Metal Film 1/4 Watt ±0.25%	1			
R62	143K	R: Metal Film 1/4 Watt ±0.25%	1			
R63	14.3K	R: Metal Film 1/4 Watt ±0.25%	1			
R64	2.87K	R: Metal Film 1/4 Watt ±0.25%	1			
R65	576Ω	R: Metal Film 1/2 Watt ±0.25%	1			
R66	2K	R: Metal Glaze 1/4 Watt ±5%	4			
R67	240K	R: Metal Glaze 1/4 Watt ±5%	2			
R68	10K	R: Variable 1/4 Watt ±20%	6			
R69-R70	100K	R: Metal Glaze 1/4 Watt ±5%	9			
R71	1.5K	R: Metal Glaze 1/4 Watt ±5%				
R72	470Ω	R: Metal Glaze 1/4 Watt ±5%	4			
R73	10Ω	R: Metal Glaze 1/4 Watt ±5%				
R74	100K	R: Metal Glaze 1/4 Watt ±5%				
R75	10K	R: Variable 1/4 Watt ±20%				
R76	240K	R: Metal Glaze 1/4 Watt ±5%				
R77	2K	R: Metal Glaze 1/4 Watt ±5%				
R78-R79	62K	R: Metal Glaze 1/4 Watt ±5%	2			
R80	1.5K	R: Metal Glaze 1/4 Watt ±5%				
R81	470Ω	R: Metal Glaze 1/4 Watt ±5%				
R82	10Ω	R: Metal Glaze 1/4 Watt ±5%				
R83	100K	R: Metal Glaze 1/4 Watt ±5%				
R84	51Ω	R: Metal Glaze 1/4 Watt ±5%	2			
R85	30K	R: Metal Glaze 1/4 Watt ±5%	4			
R86	340Ω	R: Metal Film 1/4 Watt ±1%	1			
R87	432Ω	R: Metal Film 1/4 Watt ±1%	2			
R88	3.32K	R: Metal Film 1/4 Watt ±1%	1			
R89	1.1K	R: Metal Film 1/4 Watt ±1%	1			
R90	30K	R: Metal Glaze 1/4 Watt ±5%				

Table 6-3. Main Board (A1) Parts List (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
R91	75Ω	R: Metal Film 1/4 Watt ±1%	4			
R92	357Ω	R: Metal Film 1/4 Watt ±1%	1			
R93	1K	R: Metal Glaze 1/4 Watt ±5%	9			
R94	270Ω	R: Metal Glaze 1/4 Watt ±5%	2			
R95	51Ω	R: Metal Glaze 1/4 Watt ±5%				
R96-R97	5.6Ω	R: Metal Glaze 1/4 Watt ±5%				
R98	22Ω	R: Metal Glaze 1/4 Watt ±5%	3			
R99	Unassigned					
R100-R101	100Ω	R: Metal Glaze 1/4 Watt ±5%	5			
R102	49.9Ω	R: Metal Film 1/4 Watt ±1%				
R103	1K	R: Metal Film 1/4 Watt ±1%				
R104	Unassigned					
R105	1.96K	R: Metal Film 1/4 Watt ±1%				
R106	340Ω	R: Metal Film 1/4 Watt ±1%				
R107	432Ω	R: Metal Film 1/4 Watt ±1%				
R108	1K	R: Metal Glaze 1/4 Watt ±5%				
R109	39K	R: Metal Glaze 1/4 Watt ±5%	1			
R110	10K	R: Variable 1/4 Watt ±20%				
R111	100Ω	R: Metal Glaze 1/4 Watt ±5%				
R112	10Ω	R: Metal Glaze 1/4 Watt ±5%				
R113	22Ω	R: Metal Glaze 1/4 Watt ±5%				
R114	500Ω	R: Variable 1/4 Watt ±20%				
R115	2K	R: Metal Film 1/4 Watt ±1%	1			
R116	49.9Ω	R: Metal Film 1/4 Watt ±1%				
R117	2.5K	Potentiometer, Var Pulse	1	P00334025-2		
R118-R121	Unassigned					
R122	100Ω	R: Metal Film 1/4 Watt ±1%	1			
R123	Unassigned					
R124	500Ω	Potentiometer, Output Adjust	1	P00334021		
R125	44.2Ω	R: Metal Film 1/4 Watt ±1%				
R126	150Ω	R: Metal Glaze 1/4 Watt ±5%	1			
R127	240Ω	R: Metal Glaze 1/4 Watt ±5%	3			
R128	2.2K	R: Metal Glaze 1 Watt ±5%	3			
R129	62Ω	R: Metal Glaze 1/4 Watt ±5%	2			
R130	4.7K	R: Metal Glaze 1/4 Watt ±5%				
R131	62Ω	R: Metal Glaze 1/4 Watt ±5%				
R132	2.2K	R: Metal Glaze 1 Watt ±5%				
R133	270Ω	R: Metal Glaze 1/4 Watt ±5%	2			
R134	910Ω	R: Metal Glaze 1/4 Watt ±5%				
R135	330Ω	R: Metal Glaze 1/4 Watt ±5%	3			
R136	6.2K	R: Metal Glaze 1/4 Watt ±5%	5			
R137	4.7K	R: Metal Glaze 1/4 Watt ±5%				

Table 6-3. Main Board (A1) Parts List (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
R138	6.2K	R: Metal Glaze 1/4 Watt ±5%	4			
R139	330Ω	R: Metal Glaze 1/4 Watt ±5%				
R140	910Ω	R: Metal Glaze 1/4 Watt ±5%				
R141-R142	110Ω	R: Metal Glaze 1/4 Watt ±5%	5			
R143	82Ω	R: Metal Glaze 1/4 Watt ±5%				
R144	82Ω	R: Metal Glaze 1/4 Watt ±5%				
R145	806Ω	R: Metal Film 1/4 Watt ±1%	1			
R146	249Ω	R: Metal Film 1/4 Watt ±1%	1			
R147	12K	R: Metal Glaze 1/4 Watt ±5%	1			
R148	50K	R: Variable 1/4 Watt ±20%				
R149-R150	110Ω	R: Metal Glaze 1/4 Watt ±5%				
R151	11Ω	R: Metal Glaze 1/4 Watt ±5%	1			
R152	250Ω	R: Variable 1/4 Watt ±20%	1			
R153-R154	39Ω	R: Metal Glaze 1/4 Watt ±5%	2			
R155	22Ω	R: Metal Glaze 1 Watt ±5%	2			
R156-R157	5.6Ω	R: Metal Glaze 1/4 Watt ±5%	2			
R158	22Ω	R: Metal Glaze 1 Watt ±5%				
R159-R160	100Ω	R: Metal Film 1 Watt ±0.1%	2			
R161-R162	96.25Ω	R: Metal Film 1/4 Watt ±0.1%	2			
R163	71.16Ω	R: Metal Film 1/4 Watt ±0.1%				
R164	4.7K	R: Metal Glaze 1/4 Watt ±5%				
R165	1.1K	R: Metal Glaze 1/4 Watt ±5%	3			
R166	5.1K	R: Metal Glaze 1/4 Watt ±5%	1			
R167	7.5K	R: Metal Glaze 1/4 Watt ±5%	2			
R168	1K	R: Metal Glaze 1/4 Watt ±5%				
R169	1K	R: Metal Glaze 1/4 Watt ±5%				
R170	2K	R: Metal Glaze 1/4 Watt ±5%	3			
R171	5K	R: Variable 1/4 Watt ±20%				
R172	10K	R: Metal Glaze 1/4 Watt ±5%	11			
R173	1K	R: Metal Glaze 1/2 Watt ±5%				
R174	510Ω	R: Metal Glaze 1/4 Watt ±5%	3			
R175	2K	R: Metal Glaze 1/4 Watt ±5%				
R176	1K	R: Metal Glaze 1/4 Watt ±5%				
R177	510Ω	R: Metal Glaze 1/4 Watt ±5%				
R178	2.5K	Potentiometer, Phase	1	P00334029		
R179	390K	R: Metal Glaze 1/4 Watt ±5%	1			
R180	68K	R: Metal Glaze 1/4 Watt ±5%	2			
R181	10K	R: Metal Glaze 1/4 Watt ±5%				
R182	7.5K	R: Metal Glaze 1/4 Watt ±5%	3			
R183	68K	R: Metal Glaze 1/4 Watt ±5%				
R184	510Ω	R: Metal Glaze 1/4 Watt ±5%				
R185	1.8K	R: Metal Glaze 1/4 Watt ±5%				

Table 6-3. Main Board (A1) Parts list (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
R186	1.5K	R: Metal Glaze 1/4 Watt ±5%				
R187	750Ω	R: Metal Glaze 1/4 Watt ±5%				
R188	5.1K	R: Metal Glaze 1/4 Watt ±5%	2			
R189	1K	R: Variable 1/4 Watt ±20%	1			
R190	1.8K	R: Metal Glaze 1/4 Watt ±5%	3			
R191	1K	R: Metal Glaze 1/4 Watt ±5%				
R192	2.7K	R: Metal Glaze 1/4 Watt ±5%				
R193	390Ω	R: Metal Glaze 1/4 Watt ±5%	2			
R194-R232	Unassigned					
R233	33K	R: Metal Glaze 1/4 Watt ±5%	2			
R234-R236	Unassigned					
R237	33K	R: Metal Glaze 1/4 Watt ±5%				
R238	4.32K	R: Metal Film 1/4 Watt ±1%	2			
R239	500Ω	R: Variable 1/4 Watt ±20%				
R240	665Ω	R: Metal Film 1/4 Watt ±1%	2			
R241	120Ω	R: Metal Glaze 1/4 Watt ±5%	2			
R242	11K	R: Metal Film 1/4 Watt ±1%	2			
R243	1.5K	R: Metal Glaze 1/4 Watt ±5%				
R244	Unassigned					
R245	7.5K	R: Metal Film 1/4 Watt ±1%	4			
R246	15K	R: Metal Film 1/4 Watt ±1%	2			
R247	25K	R: Variable 1/4 Watt ±20%				
R248	2.7K	R: Metal Glaze 1/4 Watt ±5%	2			
R249	22K	R: Metal Glaze 1/4 Watt ±5%				
R250	39K	R: Metal Glaze 1/4 Watt ±5%	2			
R251	10K	R: Variable 1/4 Watt ±20%				
R252	120Ω	R: Metal Glaze 1/4 Watt ±5%				
R253	750Ω	R: Metal Glaze 1/4 Watt ±5%				
R254	6.2K	R: Metal Glaze 1/4 Watt ±5%				
R255	7.5K	R: Metal Film 1/4 Watt ±1%				
R256	1.5K	R: Metal Glaze 1/4 Watt ±5%				
R257	Unassigned					
R258	5K	R: Variable 1/4 Watt ±20%				
R259	470Ω	R: Metal Glaze 1/4 Watt ±5%				
R260	4.32K	R: Metal Film 1/4 Watt ±1%				
R261	500Ω	R: Variable 1/4 Watt ±20%				
R262	665Ω	R: Metal Film 1/4 Watt ±1%				
R263	Unassigned					
R264	11K	R: Metal Film 1/4 Watt ±1%				

Table 6-3. Main Board (A1) Parts List (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
R265	1.5K	R: Metal Glaze 1/4 Watt ±5%				
R266	Unassigned					
R267	7.5K	R: Metal Film 1/4 Watt ±1%				
R268	15K	R: Metal Film 1/4 Watt ±1%				
R269	25K	R: Variable 1/4 Watt ±20%				
R270	22K	R: Metal Glaze 1/4 Watt ±5%				
R271	Unassigned					
R272	20K	R: Metal Glaze 1/4 Watt ±5%	3			
R273	150Ω	R: Metal Film 1/4 Watt ±1%				
R274	100Ω	R: Variable 1/4 Watt ±20%				
R275	75Ω	R: Metal Film 1/4 Watt ±1%				
R276	20K	R: Metal Glaze 1/4 Watt ±5%				
R277	Unassigned					
R278	10K	R: Metal Glaze 1/4 Watt ±5%				
R279	20K	R: Metal Glaze 1/2 Watt ±5%	2			
R280	100K	R: Metal Glaze 1/4 Watt ±5%				
R281	Unassigned					
R282	10K	R: Metal Glaze 1/4 Watt ±5%				
R283	20K	R: Metal Glaze 1/2 Watt ±5%				
R284	866Ω	R: Metal Film 1/4 Watt ±1%	1			
R285	47Ω	R: Metal Glaze 1/4 Watt ±5%	2			
R286-R287	10K	R: Metal Glaze 1/4 Watt ±5%				
R288	1.8K	R: Metal Glaze 1/4 Watt ±5%				
R289	1.2K	R: Metal Glaze 1/4 Watt ±5%				
R290	825Ω	R: Metal Film 1/4 Watt ±1%	2			
R291	560Ω	R: Metal Glaze 1/4 Watt ±5%	1			
R292	240Ω	R: Metal Glaze 1/4 Watt ±5%	1			
R293	100K	R: Metal Glaze 1/4 Watt ±5%				
R294	200Ω	R: Metal Glaze 1/4 Watt ±5%				
R295	4.7K	R: Metal Glaze 1/4 Watt ±5%				
R296	10K	R: Metal Glaze 1/4 Watt ±5%				
R297	Unassigned					
R298	510Ω	R: Metal Glaze 1 Watt ±5%				
R299-R300	1.1K	R: Metal Glaze 1/4 Watt ±5%				
R301	6.8K	R: Metal Glaze 1/4 Watt ±5%				
R302	56Ω	R: Metal Glaze 1/4 Watt ±5%	2			
R303-R304	3.3Ω	R: Carbon 1/4 Watt ±5%	2			
R305	1.5K	R: Metal Glaze 1 Watt ±5%	1			
R306	56Ω	R: Metal Glaze 1/4 Watt ±5%				
R307	10K	R: Metal Glaze 1/4 Watt ±5%				
R308	825Ω	R: Metal Film 1/4 Watt ±1%				
R309	10K	R: Metal Glaze 1/4 Watt ±5%				

Table 6-3. Main Board (A1) Parts List (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
R310	1.8K	R: Metal Glaze 1/4 Watt ±5%				
R311	1.5K	R: Metal Film 1/4 Watt ±1%	1			
R312	47Ω	R: Metal Glaze 1/4 Watt ±5%				
R313	1.6K	R: Metal Glaze 1 Watt ±5%				
R314	715Ω	R: Metal Film 1/4 Watt ±1%				
R315	2.5K	Potentiometer, Trigger Level	1	P00334029		
R316	Unassigned					
R317	3.3K	R: Metal Glaze 1/4 Watt ±5%				
R318	2.2K	R: Metal Glaze 1 Watt ±5%				
R319-R320	75Ω	R: Metal Glaze 1/4 Watt ±5%				
R321	1.47K	R: Metal Film 1/4 Watt ±1%				
R322	39K	R: Metal Glaze 1/4 Watt ±5%				
R323	10K	R: Variable 1/4 Watt ±20%				
R324	750Ω	R: Metal Glaze 1/4 Watt ±5%				
R325	6.2K	R: Metal Glaze 1/4 Watt ±5%				
R326	7.5K	R: Metal Film 1/4 Watt ±1%				
R327	1.5K	R: Metal Glaze 1/4 Watt ±5%				
R328	470Ω	R: Metal Glaze 1/4 Watt ±5%				
R329	2.7K	R: Metal Glaze 1/4 Watt ±5%				
R330-R331	10K	R: Metal Glaze 1/4 Watt ±5%				
R332-R336	Unassigned					
R337	390Ω	R: Metal Glaze 1/4 Watt ±5%				
R338	130Ω	R: Metal Glaze 1/4 Watt ±5%	2			
R339	Unassigned					
R340	449Ω	R: Metal Film 1/4 Watt ±1%	1			
R341	1K	R: Metal Film 1/4 Watt ±1%				
R342	Unassigned					
R343	130Ω	R: Metal Glaze 1/4 Watt ±5%				
R344	240Ω	R: Metal Glaze 1/4 Watt ±5%				
R345	10.20Ω	R: Metal Film 1/4 Watt ±0.1%	1			
R346-R347	40.91Ω	R: Metal Film 1/4 Watt ±0.1%	2			
R348	71.63Ω	R: Metal Film 1/4 Watt ±0.1%	1			
R349	156.1Ω	R: Metal Film 1/4 Watt ±0.1%	1			
R350	40.03Ω	R: Metal Film 1/4 Watt ±0.1%	1			
R351	10.53Ω	R: Metal Film 1/4 Watt ±0.1%	1			
R352	866Ω	R: Metal Film 1/4 Watt ±1%	1			
R353	78.7K	R: Metal Film 1/4 Watt ±1%				
R354	390Ω	R: Metal Glaze 1/4 Watt ±5%				
R355-R357	Unassigned					
R358-R359	100K	R: Metal Glaze 1/4 Watt ±5%				
R360	1K	R: Metal Glaze 1/4 Watt ±5%				
R361	100K	R: Metal Glaze 1/4 Watt ±5%				

Table 6-3. Main Board (A1) Parts List (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
R362	30K	R: Metal Glaze 1/4 Watt ±5%				
R363	2.4K	R: Metal Glaze 1/4 Watt ±5%				
R364	4.7K	R: Metal Glaze 1/4 Watt ±5%				
R365	78.7K	R: Metal Film 1/4 Watt ±1%				
R366	1K	R: Metal Glaze 1/4 Watt ±5%				
R367	50Ω	R: Variable 1/4 Watt ±20%	1			
R368	2.5K	R: Variable 1/4 Watt ±20%				
R369	1K	R: Metal Glaze 1/4 Watt ±5%				
R370	1.2K	R: Metal Glaze 1/4 Watt ±5%				
R371-R372	100Ω	R: Metal Glaze 1/4 Watt ±5%				
R373	620Ω	R: Metal Glaze 1/4 Watt ±5%				
R374	Select	R: Metal Glaze 1/4 Watt ±5%				
R375	12.4K	R: Metal Film 1/4 Watt ±1%				
R376	1.8K	R: Metal Glaze 1/4 Watt ±5%				
C1	0.1μf	C: Ceramic 100 volts +80% - 20%	55			
C2-C3	15μf	C: Electrolytic 50 volts +75% -10%	4			
C4-C7	20μf	C: Electrolytic 16 volts +75% -10%	6			
C8-C14	0.1μf	C: Ceramic 100 volts +80% -20%				
C15	500pf	C: Ceramic 1000 volts ±10%	5			
C16	20pf	C: Ceramic 1000 volts ±10%	4			
C17-C18	0.1μf	C: Ceramic 100 volts +80% -20%				
C19	500pf	C: Ceramic 1000 volts ±10%				
C20	20pf	C: Ceramic 1000 volts ±10%				
C21	100 pf	C: Ceramic 1000 volts ±10%	2			
C22	3.3pf	C: Ceramic 1000 volts ±0.5pf	4			
C23	20μf	C: Electrolytic 16 volts +75% -10%				
C24	200pf	C: Mica 500 volts ±10%	5			
C25	100pf	C: Ceramic 1000 volts ±10%				
C26	3.3pf	C: Ceramic 1000 volts ±0.5pf				
C27	20μf	C: Electrolytic 16 volts +75% -10%				
C28	200pf	C: Mica 500 volts ±10%				
C29	10μf	C: Mylar 100 volts ±5%	2			
C30	0.1μf	C: Polyester 50 volts ±2%	2			
C31	750pf	C: Mica 300 volts ±2%	1			
C32	220pf	C: Mica 300 volts ±2%	1			
C33	Select	C: Mica 500 volts ±5%	1			
C34	2.4-24.5pf	C: Variable Air Delectric	4			
C35	Unassigned					
C36	0.01μf	C: Ceramic 100 volts ±20%	7			
C37	0.1μf	C: Ceramic 100 volts +80% -20%				
C38	2.4-24.5pf	C: Variable Air Dielectric				
C39-C40	0.1μf	C: Ceramic 100 volts +80% -20%				

Table 6-3. Main Board (A1) Parts List (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
C41	Select	C: Mica (select)				
C42-C43	0.1μf	C: Ceramic 100 volts +80% -20%				
C44-C45	0.002μf	C: Ceramic 1000 volts ±20%	4			
C46-C47	0.1μf	C: Ceramic 100 volts +80% -20%				
C48	0.002μf	C: Ceramic 1000 volts ±20%				
C49-C50	0.1μf	C: Ceramic 100 volts +80% -20%				
C51	0.002μf	C: Ceramic 1000 volts ±20%				
C52-C53	0.1μf	C: Ceramic 100 volts +80% -20%				
C54	Unassigned					
C55	20μf	C: Electrolytic 20 volts +50% -10%	1			
C56	2μf	C: Electrolytic 20 volts +50% -10%	1			
C57	1μf	C: Electrolytic 20 volts +50% -10%	2			
C58	0.1μf	C: Polyester 80 volts ±10%	2			
C59	0.01μf	C: Ceramic 100 volts ±20%				
C60	0.001μf	C: Ceramic 1000 volts ±20%				
C61	200pf	C: Mica 200 volts ±10%	3			
C62	0.0047μf	C: Ceramic 25 volts ±20%	3			
C63	10μf	C: Electrolytic 20 volts +50% -10%				
C64	1μf	C: Electrolytic 20 volts +50% -10%				
C65	0.1μf	C: Polyester 80 volts ±10%				
C66	0.01μf	C: Ceramic 100 volts ±20%				
C67	1500pf	C: Mica 500 volts ±10%	1			
C68	560pf	C: Mica 500 volts ±10%	1			
C69-C72	Unassigned					
C73	0.1μf	C: Ceramic 100 volts +80% -20%				
C74	500pf	C: Ceramic 1000 volts ±10%				
C75	Unassigned					
C76-C77	0.1μf	C: Ceramic 100 volts +80% -20%				
C78-C79	47pf	C: Mica 500 volts ±10%	2			
C80-C85	Unassigned					
C86	20pf	C: Ceramic 1000 volts ±10%				
C87	75pf	C: Mica 500 volts ±10%	1			
C88	0.1μf	C: Ceramic 100 volts +80% -20%				
C89	200pf	C: Mica 200 volts ±10%				
C90	0.0047μf	C: Ceramic 25 volts ±20%				
C91	0.1μf	C: Ceramic 100 volts +80% -20%				
C92	20pf	C: Ceramic 1000 volts ±10%				
C93	500pf	C: Ceramic 1000 volts ±10%				
C94	0.1μf	C: Ceramic 100 volts +80% -20%				
C95	10pf	C: Mica 500 volts ±10%				
C96	Unassigned					
C97	0.1μf	C: Ceramic 100 volts +80% -20%				
C98	180pf	C: Mica 500 volts ±2%	1			

Table 6-3. Main Board (A1) Parts List (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
C99	0.1μf	C: Ceramic 100 volts +80% -20%				
C100	500pf	C: Ceramic 1000 volts ±10%				
C101-C105	0.1μf	C: Ceramic 100 volts +80% -20%				
C106	5pf	C: Mica 500 volts ±0.5 pf				
C107-C109	0.1μf	C: Ceramic 100 volts +80% -20%				
C110	200pf	C: Mica 500 volts ±10%				
C111	0.0047μf	C: Ceramic 25 volts ±20%				
C112	Unassigned					
C113	3.3pf	C: Ceramic 1000 volts ±0.5 pf				
C114	Select	C: Mica 500 volts (select)	1			
C115	1.8-16.7pf	C: Variable Air Dielectric				
C116	0.001μf	C: Ceramic 1000 volts ±20%				
C117	15μf	C: Electrolytic 50 volts +75% -10%				
C118-C119	0.1μf	C: Ceramic 100 volts +80% -20%				
C120	15μf	C: Electrolytic 50 volts +75% -10%				
C121-C123	0.1μf	C: Ceramic 100 volts +80% -20%				
C124	180pf	C: Mica 500 volts ±10%				
C125	0.01μf	C: Ceramic 100 volts ±20%				
C126-C129	0.1μf	C: Ceramic 100 volts +80% -20%				
C130	0.01μf	C: Ceramic 100 volts ±20%				
C131	47pf	C: Mica 500 volts ±10%	1			
C132	0.01μf	C: Ceramic 100 volts ±20%				
C133	200pf	C: Mica 500 volts ±10%	1			
C134	160pf	C: Mica 500 volts ±2%	1			
C135	0.001μf	C: Ceramic 1000 volts ±20%				
C136	Select	C: Mica 500 volts ±10%				
C137	0.01μf	C: Ceramic 100 volts ±20%				
C138	270pf	C: Mica 500 volts ±10%				
C139	10pf	C: Mica 500 volts ±10%				
Q1-Q2		TSTR: Silicon PNP	7			
Q3-Q4		TSTR: Silicon NPN	19			
Q5-Q6		TSTR: Dual N Chan JFET	3	P00347201		
Q7		TSTR: P Chan JFET	1	P00347250		
Q8		TSTR: N Chan JFET	2	P00347202		
Q9		TSTR: Silicon PNP	1	P00347100		
Q10		TSTR: Silicon NPN	1	P00347000		
Q11		TSTR: Dual N Chan JFET		P00347201		
Q12		TSTR: Silicon PNP	5	P00347101		
Q13		TSTR: Silicon PNP	3			
Q14-Q15		TSTR: Silicon PNP		P00347101		
Q16		TSTR: Silicon NPN				
Q17-Q18		TSTR: Silicon NPN		P00347001		

Table 6-3. Main Board (A1) Parts List (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
Q19-Q20		TSTR: Silicon NPN	3			
Q21		TSTR: Silicon PNP				
Q22-Q23		TSTR: Silicon NPN				
Q24		TSTR: Silicon NPN	1			
Q25		TSTR: Silicon PNP	1			
Q26-Q27		TSTR: Silicon PNP				
Q28		TSTR: N Chan JFET	1	P00347203		
Q29		TSTR: Silicon PNP		P00347101		
Q30	Unassigned					
Q31-Q34		TSTR: Silicon NPN				
Q35-Q41	Unassigned					
Q42		TSTR: Silicon NPN				
Q43	Unassigned					
Q44		TSTR: Silicon PNP	2			
Q45-Q48	Unassigned					
Q49		TSTR: Silicon NPN				
Q50		TSTR: Silicon PNP				
Q51		TSTR: Silicon PNP		P00347103		
Q52		TSTR: Silicon NPN				
Q53-Q54		TSTR: Silicon PNP		P00347103		
Q55		TSTR: Silicon NPN				
Q56	Unassigned					
Q57		TSTR: Silicon NPN				
Q58		TSTR: Silicon PNP				
Q59		TSTR: Silicon NPN				
Q60		TSTR: Silicon PNP				
Q61-Q62		TSTR: Silicon NPN				
Q63		TSTR: Silicon PNP				
Q64		TSTR: Silicon NPN				
Q65		TSTR: Silicon NPN	1			
CR1		Diode: Switching, Hot Carrier	7			
CR2-CR3		Diode: Low Leakage	5			
CR4		Diode: Switching, Hot Carrier				
CR5		Diode: Low Leakage				
CR6-CR7		Diode: Switching, Hot Carrier				
CR8		Diode: Low Leakage				
CR9	Select	Diode: Zener 400 mw ±5%	1			
CR10-CR15		Diode: Silicon	34			
CR16	12.0v	Diode: Zener 400 mw ±5%	1			
CR17-CR21		Diode: Silicon				
CR22		Diode: Low Leakage				
CR23		Diode: Switching, Hot Carrier				

Table 6-3. Main Board (A1) Parts List (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
CR24-CR25		Diode: Silicon				
CR26-CR30	Unassigned					
CR31-CR32		Diode: Silicon				
CR33	6.2v	Diode: Zener 400 mw ±5%				
CR34		Diode: Silicon				
CR35	Unassigned					
CR36-CR37		Diode: Switching, Hot Carrier	2			
CR38-CR39		Diode: Silicon				
CR40		Diode: Tunnel	2			
CR41		Diode: Silicon				
CR42	5.6v	Diode: Zener 400 mw ± 5%	1			
CR43		Diode: Silicon				
CR44	4.7v	Diode: Zener 400 mw ±5%	3			
CR45		Diode: Silicon				
CR46-CR47	4.7v	Diode: Zener 400 mw ±5%				
CR48-CR50		Diode: Silicon				
CR51	Unassigned					
CR52		Diode: Silicon				
CR53	Unassigned					
CR54	3.9v	Diode: Zener 400 mw ±5%	1			
CR55-CR57		Diode: Silicon				
CR58	3.0v	Diode: Zener 400 mw ±5%	1			
CR59		Diode: Silicon				
CR60		Diode: Tunnel				
CR61-CR62		Diode: Switching, Hot Carrier				
CR63-CR65		Diode: Silicon				
CR66-CR67	Unassigned					
CR68-CR69		Diode: Silicon				
IC1-IC4		Integrated Circuit Amp (μA709C)	9			
IC5		Integrated Circuit Array	1			
IC6		Integrated Circuit Amp (μA709C)				
IC7-IC8	Unassigned					
IC9-IC11		Integrated Circuit Amp (μA709C)				
IC12-IC13		Integrated Circuit Array	3			
IC14		Integrated Circuit Amp (μA709C)				
IC15		Integrated Circuit Array				
S1		Switch, Multiplier	1	P00334020		
S2		Switch, Waveform with Pot	1	P00334025-2		
S3		Switch, Attenuator with Pot	1	P00334021		
		Wire, Kynar 2, 24 AWG	A/R	516-061-001		
		Bead, Shielding	15			

Table 6-3. Main Board (A1) Parts List (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
TP1-TP26		Test Points				
		Cable Assembly, 29 Pin				
		Cable Assembly, 19 Pin				
TP27-TP32	Unassigned					
TP33-TP36		Test Points				
		Cable Assembly, 29 Pin				
		Cable Assembly, 19 Pin				
E49-E56, E58-E66, E73-E80		Test Points				

TABLE 6-4. AUXILIARY BOARD (A2) PARTS LIST

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
A2		P.C. Board Ass'y, Auxiliary Generator	Ref	P00334200-4		
R1-R2	249Ω	R: Metal Film 1/4 Watt ±1%	2			
R3	2.67K	R: Metal Film 1/4 Watt ±1%	2			
R4	2.5K	R: Variable ±20%	1	P00333023		
R5	300Ω	R: Metal Glaze 1/4 Watt ±5%	1			
R6-R7	250Ω	R: Variable 1/4 Watt ±20%	2			
R8	47K	R: Metal Glaze 1/4 Watt ±5%	2			
R9	511Ω	R: Metal Film 1/4 Watt ±1%	1			
R10	270Ω	R: Metal Glaze 1/4 Watt ±5%	1			
R11	10K	R: Variable 1/4 Watt ±20%	3			
R12	30Ω	R: Metal Glaze 1/4 Watt ±5%	4			
R13	1K	R: Metal Glaze 1/4 Watt ±5%	3			
R14	30Ω	R: Metal Glaze 1/4 Watt ±5%				
R15	1.2K	R: Metal Glaze 1/4 Watt ±5%	4			
R16	100Ω	R: Metal Glaze 1/4 Watt ±5%	9			
R17	1.2K	R: Metal Glaze 1 Watt ±5%	2			
R18	634Ω	R: Metal Film 1/4 Watt ±1%	1			
R19	510Ω	R: Metal Glaze 1/4 Watt ±5%	3			
R20	1.2K	R: Metal Glaze 1/4 Watt ±5%				
R21	100Ω	R: Metal Glaze 1/4 Watt ±5%				
R22	390Ω	R: Metal Glaze 1/4 Watt ±5%	2			
R23	51Ω	R: Metal Glaze 1/4 Watt ±5%	3			
R24-R25	15Ω	R: Metal Glaze 1/4 Watt ±5%	4			
R26	2.43K	R: Metal Film 1/4 Watt ±1%	2			
R27	619Ω	R: Metal Film 1/4 Watt ±1%	1			
R28	2K	R: Metal Film 1/4 Watt ±1%	2			
R29	100Ω	R: Metal Glaze 1/4 Watt ±5%				
R30	470Ω	R: Metal Glaze 1/4 Watt ±5%	4			
R31	100Ω	R: Metal Glaze 1/4 Watt ±5%				
R32	20K	R: Metal Glaze 1/4 Watt ±5%	3			
R33	3.01K	R: Metal Film 1/4 Watt ±1%	2			
R34	2K	R: Metal Film 1/4 Watt ±1%				
R35	390Ω	R: Metal Glaze 1/4 Watt ±5%				
R36	1.8K	R: Metal Glaze 1/2 Watt ±5%	1			
R37	2.43K	R: Metal Film 1/4 Watt ±1%				
R38	3.01K	R: Metal Film 1/4 Watt ±1%				
R39	39Ω	R: Metal Glaze 1/4 Watt ±5%	2			
R40-R41	10Ω	R: Metal Glaze 1/4 Watt ±5%	8			
R42	39Ω	R: Metal Glaze 1/4 Watt ±5%				
R43	107Ω	R: Metal Film 1/4 Watt ±1%	1			
R44	200Ω	R: Metal Film 1/4 Watt ±1%	2			
R45	100Ω	R: Variable 1/4 Watt ±20%	2			

Table 6-4. Auxiliary Board (A2) Parts List (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
R46	10K	R: Metal Glaze 1/4 Watt ±5%	1			
R47-R48	5.1K	R: Metal Glaze 1/2 Watt ±5%	2			
R49	4.7K	R: Metal Glaze 1/4 Watt ±5%	2			
R50	82K	R: Metal Glaze 1/4 Watt ±5%	1			
R51	1.1K	R: Metal Glaze 1/4 Watt ±5%	3			
R52	2.2K	R: Metal Glaze 1/4 Watt ±5%	9			
R53	2.7K	R: Metal Glaze 1/4 Watt ±5%	3			
R54-R59	2.2K	R: Metal Glaze 1/4 Watt ±5%				
R60-R61	200Ω	R: Metal Glaze 1/4 Watt ±5%	2			
R62	2.7K	R: Metal Glaze 1/4 Watt ±5%				
R63	470Ω	R: Metal Glaze 1/4 Watt ±5%				
R64	47K	R: Metal Glaze 1/4 Watt ±5%				
R65	750Ω	R: Metal Glaze 1/4 Watt ±5%	2			
R66	2.7K	R: Metal Glaze 1/4 Watt ±5%				
R67-R68	100Ω	R: Metal Glaze 1/4 Watt ±5%				
R69-R82	Unassigned					
R83	10K	R: Metal Film 1/4 Watt ±1%	1			
R84-R105	Unassigned					
R106	1.1K	R: Metal Film 1/4 Watt ±1%				
R107-R108	2.21K	R: Metal Film 1/4 Watt ±1%				
R109	1.1K	R: Metal Film 1/4 Watt ±1%				
R110	47.5Ω	R: Metal Film 1/4 Watt ±1%	2			
R111	Unassigned					
R112	50Ω	R: Variable 1/4 Watt ±20%				
R113	124Ω	R: Metal Film 1/4 Watt ±1%	1			
R114	49.9Ω	R: Metal Film 1/4 Watt ±1%	3			
R115	75Ω	R: Metal Film 1/4 Watt ±1%	2			
R116	150Ω	R: Metal Glaze 1/4 Watt ±5%	1			
R117-R118	4.7Ω	R: Carbon 1/4 Watt ±5%	2			
R119	22Ω	R: Metal Glaze 1/4 Watt ±5%	2			
R120	470Ω	R: Metal Glaze 1/4 Watt ±5%				
R121-R122	30Ω	R: Metal Glaze 1/4 Watt ±5%				
R123	470Ω	R: Metal Glaze 1/4 Watt ±5%				
R124-R125	10Ω	R: Metal Glaze 1/4 Watt ±5%				
R126	1.2K	R: Metal Glaze 1/4 Watt ±5%				
R127	500Ω	R: Variable 1/4 Watt ±20%	4			
R128	620Ω	R: Metal Glaze 1/4 Watt ±5%	2			
R129	43Ω	R: Metal Glaze 1/4 Watt ±5%	1			
R130	4.7K	R: Metal Glaze 1/4 Watt ±5%				
R131	Unassigned					
R132	7.5Ω	R: Metal Glaze 1/4 Watt ±5%	1			
R133	22.1Ω	R: Metal Film 1/4 Watt ±1%	1			

Table 6-4. Auxiliary Board (A2) Parts List (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
R134	39.2Ω	R: Metal Film 1/4 Watt ±1%	1			
R135	47.5Ω	R: Metal Film 1/4 Watt ±1%				
R136	130Ω	R: Metal Film 1/4 Watt ±1%	1			
R137	182Ω	R: Metal Film 1/4 Watt ±1%	1			
R138	430Ω	R: Metal Glaze 1/4 Watt ±5%	2			
R139	100Ω	R: Metal Glaze 1/4 Watt ±5%				
R140	430Ω	R: Metal Glaze 1/4 Watt ±5%				
R141	1.2K	R: Metal Glaze 1/4 Watt ±5%				
R142	500Ω	R: Variable 1/4 Watt ±20%				
R143	620Ω	R: Metal Glaze 1/4 Watt ±5%				
R144-R158	Unassigned					
R159	49.9Ω	R: Metal Film 1/4 Watt ±1%				
R160	75Ω	R: Metal Film 1/4 Watt ±1%				
R161	150Ω	R: Metal Film 1/4 Watt ±1%	1			
R162-R169	Unassigned					
R170	15Ω	R: Metal Glaze 1/4 Watt ±5%				
R171	1.6K	R: Metal Glaze 1 Watt ±5%				
R172	340Ω	R: Metal Film 1/4 Watt ±1%				
R173	15Ω	R: Metal Glaze 1/4 Watt ±5%				
R174	1K	R: Metal Glaze 1/4 Watt ±5%				
R175	51Ω	R: Metal Glaze 1/4 Watt ±5%				
R178	1.47K	R: Metal Film 1/4 Watt ±1%	5			
R179	2.5K	R: Variable 1/4 Watt ±20%	1			
R180	22Ω	R: Metal Glaze 1/4 Watt ±5%				
R181	137Ω	R: Metal Film 1/4 Watt ±1%	1			
R182	250Ω	R: Variable 1/4 Watt ±20%	1			
R183	240Ω	R: Metal Glaze 1/4 Watt ±5%				
R184	Unassigned					
R185-R186	100Ω	R: Metal Glaze 1/4 Watt ±5%				
R187	51Ω	R: Metal Glaze 1/4 Watt ±5%				
R188	Unassigned					
R189	2.67K	R: Metal Film 1/4 Watt ±1%				
R190	511Ω	R: Metal Film 1/4 Watt ±1%				
R191	137Ω	R: Metal Film 1/4 Watt ±1%				
R192	Unassigned					
R193	49.9Ω	R: Metal Film 1/4 Watt ±1%				
R194-R196	Unassigned					
R197	4.7K	R: Metal Glaze 1/4 Watt ±5%				
R198-R199	6.8K	R: Metal Glaze 1/4 Watt ±5%	2			
R200-R201	10Ω	R: Metal Glaze 1/4 Watt ±5%	2			

Table 6-4. Auxiliary Board (A2) Parts List (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	:EC P/N	MFR	MFR P/N
R202	61.9Ω	R: Metal Film 1/4 Watt ±1%	1			
R203	150Ω	R: Metal Film 1/4 Watt ±1%	1			
R204-R205	1K	R: Metal Film 1/4 Watt ±1%	1			
R206	180K	R: Metal Glaze 1/4 Watt ±5%				
R207	3K	R: Metal Glaze 1/4 Watt ±5%				
R208-R209	100K	R: Metal Glaze 1/4 Watt ±5%	2			
R210	1K	R: Metal Glaze 1/4 Watt ±5%				
C1-C2	0.1µf	C: Ceramic 100 volts +80% -20%	33			
C3	0.01µf	C: Ceramic 100 volts ±20%	2			
C4	0.1µf	C: Ceramic 100 volts +80% -20%				
C5	2.4-24.5pf	C: Variable Air Dielectric	2			
C6-C7	0.1µf	C: Ceramic 100 volts +80% -20%				
C8	10pf	C: Ceramic 1000 volts ±10%	2			
C9-C13	0.1µf	C: Ceramic 100 volts +80% -20%				
C14	Unassigned					
C15	0.1µf	C: Ceramic 100 volts +80% -20%				
C16-C19	50pf	C: Mica 500 volts ±10%	4			
C20	20µf	C: Electrolytic 16 volts +75% -10%	5			
C21-C29	Unassigned					
C30-C34	0.1µf	C: Ceramic 100 volts +80% -20%				
C35-C36	100pf	C: Ceramic 1000 volts ±10%	4			
C37-C40	0.1µf	C: Ceramic 100 volts +80% -20%				
C41	Unassigned					
C42	0.001µf	C: Ceramic 100 volts ±20%	1			
C43	2.4-24.5pf	C: Variable Air Dielectric				
C44	20pf	C: Mica 500 volts ±10%	1			
C45	0.01µf	C: Ceramic 100 volts ±20%				
C46-C47	0.1µf	C: Ceramic 100 volts +80% -20%				
C48	10pf	C: Ceramic 1000 volts ±10%	1			
C49-C50	20µf	C: Electrolytic 16 volts +75% -10%				
C51	Unassigned					
C52-C56	0.1µf	C: Ceramic 100 volts +80% -20%				
C57	Unassigned					
C58	15µf	C: Electrolytic 50 volts +75% -10%	2			
C59-C60	20µr	C: Electrolytic 16 volts +75% -10%				
C61-C64	0.1µf	C: Ceramic 100 volts +80% -20%				
C65-C67	Unassigned					
C68	Select	C: Mica 500 volts (select)				
C69	Unassigned					
C70-C71	100pf	C: Ceramic 1000 volts ±10%	2			
C72	39pf	C: Mica 500 volts ±10%	1			
C73-C74	0.1µf	C: Ceramic 100 volts +80% -20%				

Table 6-4. Auxiliary Board (A2) Parts List (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
C75	15μf	C: Electrolytic 50 volts +75% -10%				
Q1-Q2		TSTR: Silicon NPN	4			
Q3-Q4	Unassigned					
Q5		TSTR: Silicon PNP	3	P00347101		
Q6-Q7		TSTR: Silicon NPN				
Q8		TSTR: Silicon PNP		P00347101		
Q9	Unassigned					
Q10-Q11		TSTR: Silicon NPN	4			
Q12		TSTR: Silicon NPN	18			
Q13		TSTR: Silicon PNP	14			
Q14		TSTR: Silicon NPN				
Q15		TSTR: Unijunction	1			
Q16		TSTR: Silicon NPN				
Q17-Q18	Unassigned					
Q19		TSTR: Silicon PNP	2			
Q20		TSTR: Silicon NPN				
Q21		TSTR: Silicon NPN				
Q22-Q23		TSTR: Silicon PNP				
Q24-Q25		TSTR: Silicon NPN				
Q26		TSTR: Silicon PNP				
Q27		TSTR: Silicon NPN				
Q28-Q34		TSTR: Silicon PNP				
Q35-Q42		TSTR: Silicon NPN				
Q43-Q44		TSTR: Silicon PNP				
Q45-Q52	Unassigned					
Q53-Q54		TSTR: Silicon NPN	2			
Q55		TSTR: Silicon PNP		P00347101		
Q56		TSTR: Silicon NPN				
Q57		TSTR: Silicon PNP				
Q58		TSTR: Silicon NPN				
Q59		TSTR: Silicon PNP				
Q60-Q61		TSTR: Silicon NPN				
CR1-CR6		Diode: Silicon	30			
CR7	Unassigned					
CR8-CR12		Diode: Silicon				
CR13	Unassigned					
CR14-CR26		Diode: Silicon				
CR27		Diode: Silicon 100 volts, 1A	1			
CR28-CR35	Unassigned					
CR36		Diode: Silicon				
CR37-CR38	Unassigned					
CR39-CR40		Diode: Silicon				

Table 6-4. Auxiliary Board (A2) Parts List (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
CR42	Unassigned					
CR43		Diode: Silicon				
CR44	Unassigned					
CR45-CR46		Diode: Silicon				
IC1-IC2		Integrated Circuit (μA710C)	2			
IC3-IC7		Integrated Circuit, TTL Logic DIP	5			
L1-L2	10μh	Inductor, Fixed ±10%	2			
L3	3.9μh	Inductor, Fixed ±10%	1			
RN1-RN2		Resistor Network	2	P00334023		
		Bead, Shielding	6			
TP1-TP18		Test Points				
TP19-TP26	Unassigned					
TP27-TP35		Test Points				
E1-E6		Contact				
E7-E10	Unassigned					
E11-E15		Contact				
E1-E6		Test Points				
E7-E10	Unassigned					
E11-E38		Test Points				
S1		Switch, Offset with Pot	1	P00333073		
S2		Switch, Mode	1	P00334030		
S3		Switch, Reset, Cal, Trig, Slipe, Man, Pwr	1	P00334031		
DS1		Lamp	1	P00347900		
J1-J2		Connector, 19 Pin	2			
		Receptacle, Bulkhead, BNC, Round Mtg. Flange (used with Basic Model)	7	Y70B3000		
		Wire, Kynar 2, 24 AWG	A/R	516-061-001		
		Coax Cable	A/R			
		Wire, 24 AWG, T/P, WHT/BLK	A/R	515-020-249		
		Wire, 22 AWG, T/P, WHT/BLK	A/R	515-020-229		
P4		Pin, Housing	1			
P4		Pin, 22-18 AWG	2			
		Cable Assembly, 19 Pin	2	P00333600-3		

TABLE 6-5. POWER SUPPLY BOARD (A3) PARTS LIST

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
A3		P.C.Board Ass'y, Power Supply	Ref	P00334300-1		
		P.C.Board Ass'y, Power Supply	Ref	P00334300-2		
R1-R2	4.3Ω	R: Carbon 1/4 Watt ±5%	4			
R3	680Ω	R: Metal Glaze 1/4 Watt ±5%	6			
R4	1.3K	R: Metal Glaze 1/2 Watt ±5%	2			
R5	2K	R: Metal Glaze 1/4 Watt ±5%	6			
R6	1.5K	R: Metal Glaze 1/4 Watt ±5%	6			
R7	2.7K	R: Metal Glaze 1/4 Watt ±5%	6			
R8-R9	10K	R: Metal Film 1/4 Watt ±0.25%	2			
R10	680Ω	R: Metal Glaze 1/4 Watt ±5%				
R11	1.3K	R: Metal Glaze 1/2 Watt ±5%				
R12	2K	R: Metal Glaze 1/4 Watt ±5%				
R13	1.5K	R: Metal Glaze 1/4 Watt ±5%				
R14	2.7K	R: Metal Glaze 1/4 Watt ±5%				
R15	12.4K	R: Metal Film 1/4 Watt ±0.25%	1			
R16	6190Ω	R: Metal Film 1/4 Watt ±0.25%	1			
R17-R18	4.3Ω	R: Carbon 1/4 Watt ±5%				
R19	Unassigned					
R20	1.0Ω	R: Wirewound 2 Watt ±5%	2			
R21	680Ω	R: Metal Glaze 1/4 Watt ±5%				
R22	390Ω	R: Metal Glaze 1/2 Watt ±5%	2			
R23	2K	R: Metal Glaze 1/4 Watt ±5%				
R24	1.5K	R: Metal Glaze 1/4 Watt ±5%				
R25	3K	R: Metal Glaze 1/4 Watt ±5%	1			
R26	2.7K	R: Metal Glaze 1/4 Watt ±5%				
R27	2K	R: Metal Film 1/4 Watt ±1%	1			
R28	1K	R: Variable 1/4 Watt ±20%	1			
R29	2.67K	R: Metal Film 1/4 Watt ±1%	1			
R30	680Ω	R: Metal Glaze 1/4 Watt ±5%				
R31	390Ω	R: Metal Glaze 1/2 Watt ±5%				
R32	2K	R: Metal Glaze 1/4 Watt ±5%				
R33	1.5K	R: Metal Glaze 1/4 Watt ±5%				
R34	2.7K	R: Metal Glaze 1/4 Watt ±5%				
R35-R36	4750Ω	R: Metal Film 1/4 Watt ±0.25%	2			
R37	1.0Ω	R: Wirewound 2 Watt ±5%				
R38	Unassigned					
R39	3.3Ω	R: Carbon 1/4 Watt ±5%	1			
R40	3.0Ω	R: Carbon 1/4 Watt ±5%				
R41	680Ω	R: Metal Glaze 1/4 Watt ±5%				
R42	160Ω	R: Metal Glaze 1/4 Watt ±5%	2			
R43	2K	R: Metal Glaze 1/4 Watt ±5%				
R44	1.5K	R: Metal Glaze 1/4 Watt ±5%				

Table 6-5. Power Supply Board (A3) Parts List (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
R45	2.7K	R: Metal Glaze 1/4 Watt ±5%				
R46-R47	2210Ω	R: Metal Film 1/4 Watt ±0.25%	2			
R48	680Ω	R: Metal Glaze 1/4 Watt ±5%				
R49	160Ω	R: Metal Glaze 1/4 Watt ±5%				
R50	2K	R: Metal Glaze 1/4 Watt ±5%				
R51	1.5K	R: Metal Glaze 1/4 Watt ±5%				
R52	2.7K	R: Metal Glaze 1/4 Watt ±5%				
R53	5620Ω	R: Metal Film 1/4 Watt ±1%	1			
R54	500Ω	R: Variable 1/4 Watt ±20%	1			
R55	2210Ω	R: Metal Film 1/4 Watt ±1%	1			
R56-R57	5.1Ω	R: Carbon 1/4 Watt ±5%	2			
R58	Unassigned					
R59-R60	5.1K	R: Metal Glaze 1/2 Watt ±5%	2			
R61-R66	91Ω	R: Metal Glaze 1/4 Watt ±5%	6			
R67-R68	220K	R: Metal Glaze 1/4 Watt ±5%	2			
R69	68K	R: Metal Glaze 1/4 Watt ±5%	1			
R70	120K	R: Metal Glaze 1/4 Watt ±5%	1			
R71	30K	R: Metal Glaze 1/4 Watt ±5%	1			
R72	43K	R: Metal Glaze 1/4 Watt ±5%	1			
C1	1250μf	C: Electrolytic 50 volts +150% -10%	2			
C2	200pf	C: Mica 500 volts ±20%	6			
C3	20pf	C: Mica 500 volts ±10%	6			
C4	100μf	C: Electrolytic 50 volts +100% -10%	4			
C5	0.1μf	C: Ceramic 100 volts +80% -20%	14			
C6	1250μf	C: Electrolytic 50 volts +150% -10%				
C7	20pf	C: Mica 500 volts ±10%				
C8	200pf	C: Mica 500 volts ±10%				
C9	100μf	C: Electrolytic 50 volts +100% -10%				
C10	0.1μf	C: Ceramic 100 volts +80% -20%				
C11	200pf	C: Mica 500 volts ±10%				
C12	20pf	C: Mica 500 volts ±10%				
C13	0.1μf	C: Ceramic 100 volts +80% -20%				
C14	100μf	C: Electrolytic 50 volts +100% -10%				
C15	0.1μf	C: Ceramic 100 volts +80% -20%				
C16-C17	1500μf	C: Electrolytic 25 volts +150% -10%	2			
C18	20pf	C: Mica 500 volts ±10%				
C19	200pf	C: Mica 500 volts ±10%				
C20	100μf	C: Electrolytic 50 volts +100% -10%				
C21	0.1μf	C: Ceramic 100 volts +80% -20%				
C22	2500μf	C: Electrolytic 15 volts +150% -10%	2			
C23	2pf	C: Mica 500 volts ±0.5 pf	2			
C24	200pf	C: Mica 500 volts ±10%				

Table 6-5. Power Supply Board (A3) Parts List (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
C25	100μf	C: Electrolytic 15 volts +150% -10%	2			
C26	0.1μf	C: Ceramic 100 volts +80% -20%				
C27	2500μf	C: Electrolytic 15 volts +150% -10%				
C28	2pf	C: Mica 500 volts &0.5pf				
C29	200pf	C: Mica 500 volts ±10%				
C30	100μf	C: Electrolytic 15 volts +150% -10%				
C31-C32	0.1μf	C: Ceramic 100 volts +80% -20%				
C33-C38	0.1μf	C: Ceramic 100 volts +80% -20%				
C39-C44	0.01μf	C: Ceramic 100 volts ±20%	6			
Q1		TSTR: Silicon PNP	3			
Q2		TSTR: Silicon PNP	2			
Q3		TSTR: Silicon NPN	2			
Q4		TSTR: Silicon PNP				
Q5		TSTR: Silicon NPN				
Q6		TSTR: Silicon NPN	3			
Q7		TSTR: Silicon PNP				
Q8		TSTR: Silicon PNP	4			
Q9		TSTR: Silicon NPN	4			
Q10		TSTR: Silicon PNP				
Q11		TSTR: Silicon NPN				
Q12		TSTR: Silicon NPN				
Q13		TSTR: Silicon PNP				
Q14		TSTR: Silicon PNP				
Q15		TSTR: Silicon NPN				
Q16		TSTR: Silicon PNP				
Q17		TSTR: Silicon NPN				
Q18		TSTR: Silicon NPN				
CR1-CR4		Diode: Silicon 100 volts PRV 1 Amp	12			
CR5-CR10		Diode: Silicon	23			
CR11-CR14		Diode: Silicon 100 volts PRV 1 Amp				
CR15-CR19		Diode: Silicon				
CR20		Diode: Zener 6.2 volts 500 mw ±5%	1			
CR21-CR26		Diode: Silicon				
CR27-CR30		Diode: Silicon 100 volts PRV 1 Amp				
CR31-CR36		Diode: Silicon				
IC1-IC6		Integrated Circuit (μA709C) DIP	6			
S1		Switch, Slide, DPDT	1			
T1		Transformer, Power	1	P00333420		
F1	1/2 Amp/ 115v - 1/4 Amp/ 230v	Fuse, 3AG SLO-BLO	1			

Table 6-5. Power Supply Board (A3) Parts List (Continued)

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
J3		Connector, P.C.Board,Double Readout	1			
		Cord, Power, 3 Conductor	1			
J4		Socket, 18-22 AWG	2			
J4		Housing	1			
TP1-TP7		Test Points	7			
		Receptacle, Bulkhead, BNC, Round Mtg. Flange (used with Rack Mount)	9			
		Wire, 22 AWG T/P WHT/BLK	A/R	515-020-229		
		Coax Cable	A/R			
		Contact	18			
		Ferrule, Outer	1	371-392-175		
		Ferrule, Inner	1	371-391-109		
		Wire, 22AWG, Twisted Shielded Pair, WHT/BLK		516-002-220		

TABLE 6-6. MECHANICAL PARTS LIST

REF DESIG	VALUE	DESCRIPTION	T.Q.	IEC P/N	MFR	MFR P/N
		Fuse Post, Miniature, 3AG	1			
		Bushing, Strain Relief, Black	1			
		Stand Off, 7/8", 4-40	2			
		Shaft Extender	1	P00334028		
		Bracket, Pot Mounting	1	P00334022		
		Shield, Attenuator Switch	2	P00334047		
		Rod, Support	2	P00334050		
		Sub-Panel, Lower	1	P00334044		
		Sub-Panel, Upper	1	P00334045-2		
		Ball Drive, 6:1	1	P00333029		
		Nut Plate, Floating, Right Angle	6			
		Stand Off, Hex Swage	2	P00333320		
		Pad, Beige	2			
		Spacer	10	464-099-001		
		Spacer, #4 x 0.25 LG				
		Thermal Link, A2-Q1 & A2-Q2	1			
		Heatsinks, A3: -Q1, -Q6, -Q7, -Q12, -Q13 & -Q18	6	P00333540-1		
		Heat Dissipators, A1-Q19 & A1-Q20	2			
		Heat Dissipators, A1-Q24 & A1-Q25	2			
		Heat Dissipators, A1-Q21 & A1-Q22	2			
		Grommet, Rubber	1			
		Lug	7	371-203-012		
		Set Screw, Cres with Cup Point	1			
		Set Screw, Cres with Cup Point	1			
		Heat Dissipator, A1-Q11 & A1-IC5	2			
		Heatsink	1	P00333540-3		
		Stand Off, Aluminum, 3/16 Dia. x 0.312 LG	2			
		Transipad, A1-Q21 & A1-Q22	2	464-002-020		
		Pin, 0.039 Dia. x 3/8 LG	1			

Section VII
CIRCUIT DIAGRAMS

7-1. INTRODUCTION

This section contains the functional block diagram, detailed schematic diagrams, and component location diagrams and tables for the Function Generator Models F52/F53.

7-2. FUNCTIONAL BLOCK DIAGRAM

Figure 7-1 is a functional block diagram of the entire function generator showing important test points and the variable components used in the adjustment and calibration procedure.

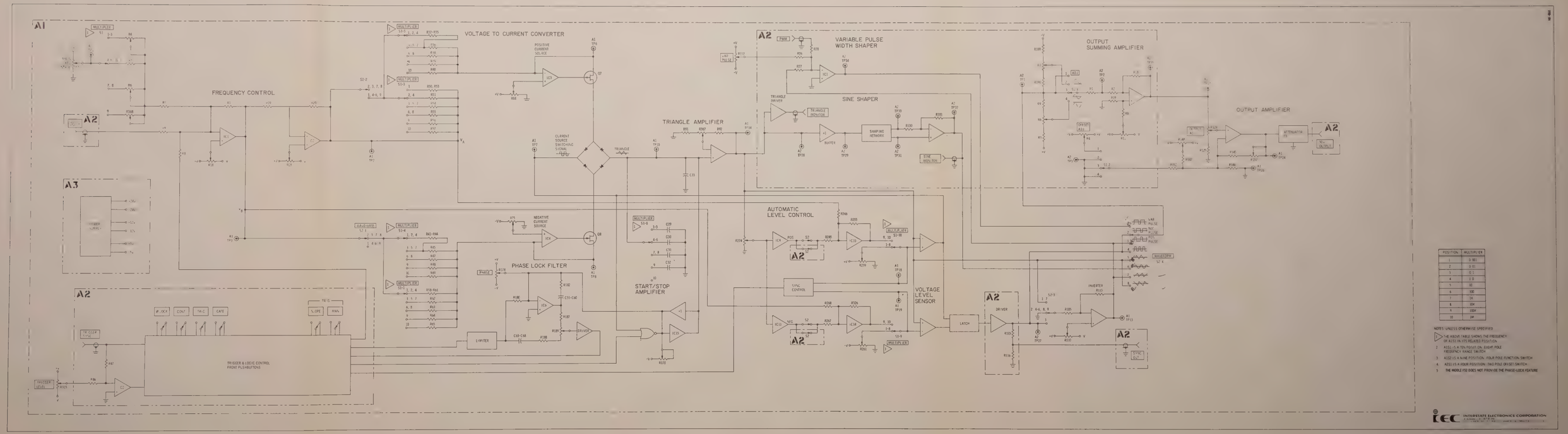
7-3. SCHEMATIC DIAGRAMS

Figures 7-3, 7-5, and 7-7 are detailed schematic diagrams of the circuits in the function generator. Special emphasis has been placed on illustrating all integrated circuit packages in their top view position and actual physical appearance. All wafer-type switches are physically illustrated with their connecting components. An overall unit schematic diagram, showing the major signal path in heavy lines, is also supplied, in separate cover, with this manual. Included on this complete schematic are test point waveforms and measurements, test point locations, and adjustment locations.

7-4. COMPONENT LOCATION DIAGRAMS

Figures 7-2, 7-4, and 7-6 are component location (assembly) diagrams. These assembly diagrams, and tables 7-1 through 7-3, will assist in the identification and location of components and test points on each board.

Q24
2N2219
Q25
2N2905



POSITION	MULTIPLIER
1	0.001
2	0.01
3	0.1
4	1.0
5	10
6	100
7	1K
8	10K
9	100K
10	1M

NOTES: UNLESS OTHERWISE SPECIFIED

1. THE ABOVE TABLE SHOWS THE FREQUENCY OF A2S1 IN ITS RELATED POSITION.
2. A2S1 IS A TEN-POSITION, EIGHT-POLE FREQUENCY RANGE SWITCH.
3. A2S2 IS A NINE-POSITION, FOUR-POLE FUNCTION SWITCH.
4. A2S3 IS A FOUR-POSITION, TWO-POLE OFFSET SWITCH.
5. THE MODEL F53 DOES NOT PROVIDE THE PHASE-LOCK FEATURE.

Figure 7-1. Functional Block Diagram

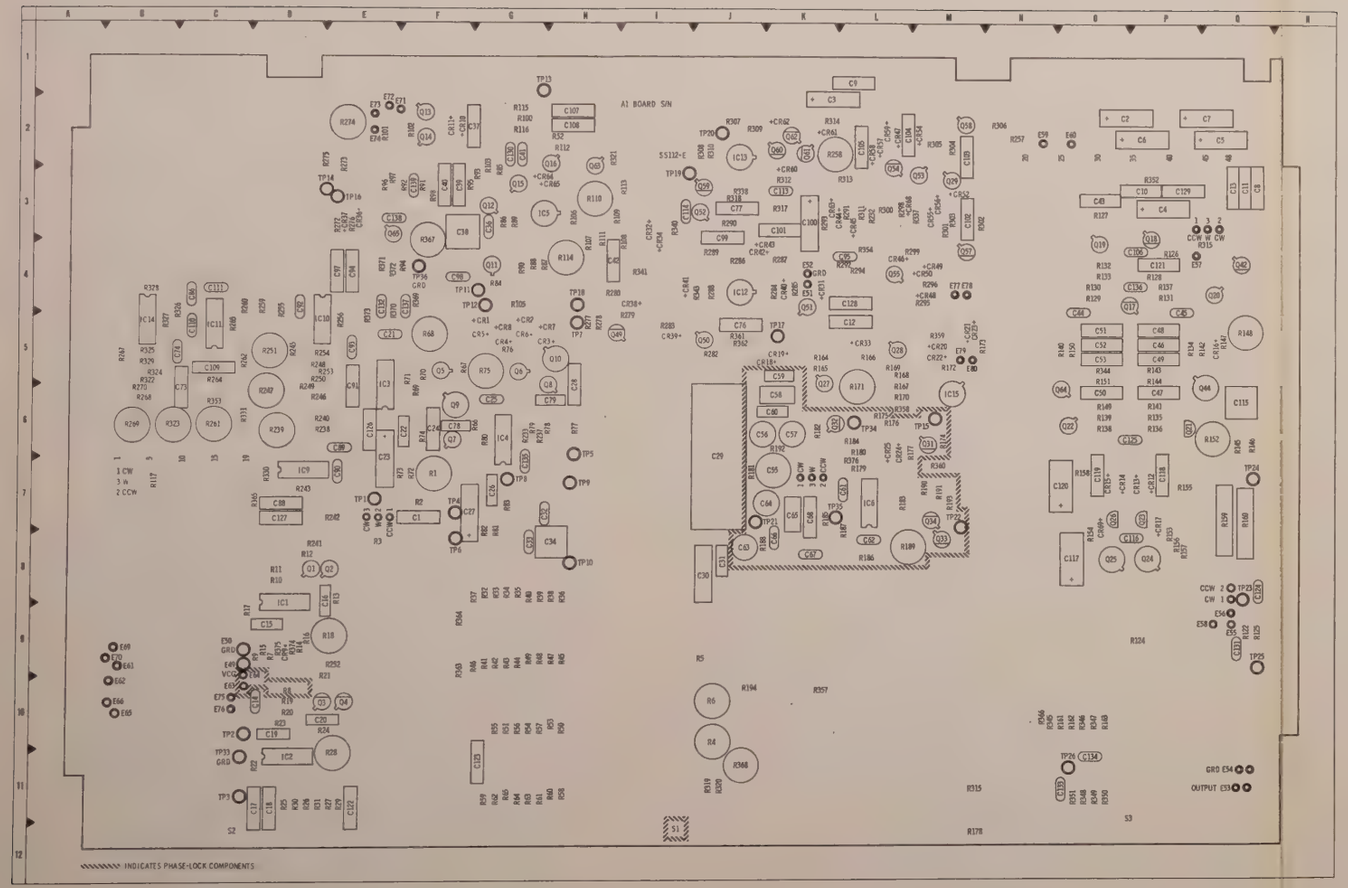
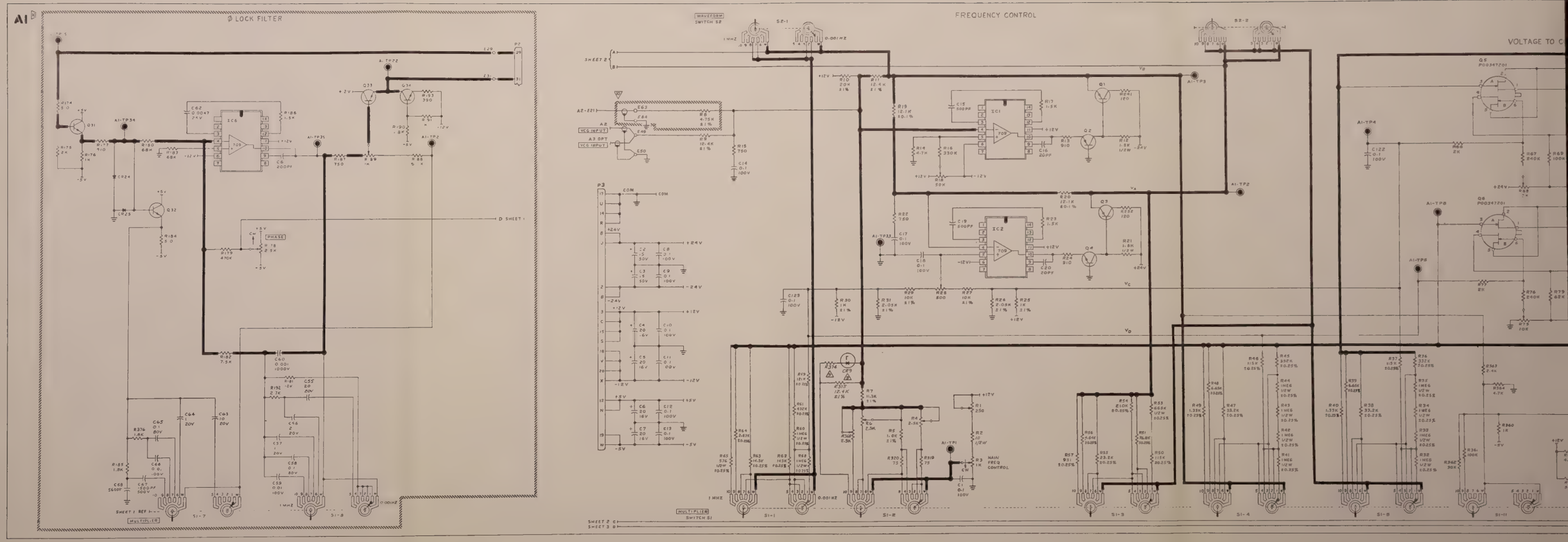


TABLE 7-1. MAIN BOARD (A1) COMPONENT LOCATIONS

REF DESIG	ZONE	REF DESIG	ZONE	REF DESIG	ZONE	REF DESIG	ZONE	REF DESIG	ZONE	REF DESIG	ZONE	REF DESIG	ZONE	REF DESIG	ZONE
C1	F7	C79	L4	C365	L2	Q61	K2	R76	G5	R362	Q10	R391	L2	TP4	F7
C2	G3	C97	E4	C366	L3	Q63	K2	R77	G5	R363	K3	R393	L4	TP5	H6
C3	E2	C98	F4	C367	L3	Q65	H2	R78	G6	R365	K3	R395	L2	TP6	F5
C4	F3	C99	J3	C368	M4	Q66	G4	R79	G6	R366	L3	R396	L3	TP7	H5
C5	G3	C100	E3	C369	M4	Q68	G5	R80	G6	R367	L6	R395	M4	TP8	G7
C6	F3	C101	E3	C370	M4	R1	F7	R81	G6	R368	L5	R396	M4	TP9	H7
C7	G2	C102	M3	C372	M5	R2	F7	R82	G5	R369	L5	R398	L3	TP10	H6
C8	G3	C103	M2	C374	M5	R3	E8	R83	G7	R370	L6	R399	L4	TP11	G4
C9	L1	C104	L2	C375	M5	R4	J10	R84	G4	R371	L6	R300	L2	TP12	G4
C10	F2	C105	L2	C376	M5	R5	J9	R85	G3	R372	M5	R301	M3	TP13	G1
C11	G3	C106	G3	C437	L3	R6	J10	R86	G2	R373	M5	R302	M2	TP14	E3
C12	L5	C107	M2	C438	L2	R7	D9	R87	G4	R374	M6	R303	M2	TP15	M8
C13	G3	C108	M3	C439	L2	R8	D10	R88	G4	R375	L6	R304	M2	TP16	E3
C14	D10	C109	C5	C440	K3	R9	D9	R89	G3	R376	L6	R305	M2	TP17	K3
C15	D9	C110	C5	C441	K2	R10	D8	R90	G4	R377	L6	R306	M3	TP18	H4
C16	E8	C111	C4	C442	K2	R11	D8	R91	F3	R378	K6	R307	J2	TP19	L3
C17	D11	C113	K2	C443	K2	R12	D8	R92	F3	R379	L7	R308	J2	TP20	J3
C18	D11	C114	L3	C444	G3	R13	E8	R93	G3	R380	L6	R309	J2	TP21	J7
C19	D10	C115	G4	C445	H3	R14	D4	R94	E4	R381	J7	R310	J2	TP22	M7
C20	D10	C116	F6	C448	L3	R15	D9	R95	F3	R382	K6	R311	L3	TP23	G9
C21	E5	C117	G6	C449	G7	R16	D9	R96	E3	R383	L7	R312	E3	TP24	G7
C22	F6	C118	F7	IC1	D8	R17	C9	R97	E3	R384	L6	R313	L3	TP25	G9
C23	E6	C119	G7	IC2	D11	R18	E9	R98	F3	R385	K7	R314	K3	TP26	C11
C24	F6	C120	G7	IC3	L5	R19	D10	R100	G2	R386	L8	R315	M11	TP32	C11
C25	G6	C121	F4	IC4	G4	R20	D10	R101	E3	R387	L8	R317	K3	TP34	L6
C26	G7	C122	E11	IC5	G3	R21	E10	R102	F3	R388	J8	R318	J2	TP35	K7
C27	F7	C123	G11	IC6	L4	R22	D11	R103	G2	R389	L8	R319	J2	TP36	A4
C28	H3	C124	G9	IC7	D7	R23	D10	R104	G4	R390	M7	R320	J11	TP37	F7
C29	J6	C125	F6	IC10	D8	R24	E10	R105	H3	R391	M7	R321	K3	TP38	C9
C30	J8	C126	F5	IC11	C3	R25	D11	R107	H4	R392	K6	R322	K3	TP39	C9
C31	J8	C127	D7	IC12	J4	R26	D11	R108	G3	R393	M7	R323	K4	TP40	E4
C32	M7	C129	F3	IC13	J2	R27	E11	R109	H5	R394	K6	R324	L5	TP41	C11
C33	G4	C130	G3	IC14	B5	R28	E11	R110	H3	R395	M7	R325	B6	TP42	C10
C34	H8	C131	G9	IC15	M6	R29	E11	R111	H3	R396	D6	R326	C9	TP43	C10
C35	G9	C132	E5	Q1	D8	R30	D11	R112	H3	R397	D6	R327	B5	TP44	C9
C36	F7	C133	G11	Q2	E5	R31	D11	R113	J2	R398	D6	R328	B4	TP45	G3
C37	F6	C134	G11	Q3	E10	R32	G8	R114	M4	R399	D6	R329	B5	TP46	C3
C38	F6	C135	G7	Q4	E10	R33	G8	R115	G2	R300	D7	R330	G5	TP47	H3
C39	F6	C136	G5	Q5	F6	R34	G8	R116	G2	R301	C6	R331	C6	TP48	C3
C41	G2	C137	E3	Q6	G5	R35	G8	R117	B7	R302	D7	R332	C6	TP49	B9
G2	H4	C138	E3	Q7	F6	R36	H8	R122	G9	R303	C6	R333	J2	TP50	B10
G3	G5	C139	F5	Q8	H6	R37	B7	R123	F9	R304	C6	R334	C6	TP51	C10
G4	G5	C140	G5	Q9	F6	R38	H8	R125	G9	R305	C5	R335	B6	TP52	C8
G5	F5	C82	G5	Q10	H5	R39	G8	R126	F9	R306	C5	R336	B6	TP53	B10
G6	F5	C83	H5	Q11	G4	R40	G8	R127	G9	R307	C5	R337	B6	TP54	B9
G7	F6	C84	G5	Q12	G3	R41	G8	R128	G4	R308	C5	R338	B6	TP55	B9
G8	F5	C85	G5	Q13	G3	R42	G8	R129	G4	R309	C5	R339	B6	TP56	C10
G9	F5	C86	G5	Q14	F2	R43	G4	R130	G4	R310	C5	R340	B6	TP57	C10
G10	G6	C87	G5	Q15	G3	R44	G9	R131	G4	R311	C5	R341	B6	TP58	C10
G11	G5	C88	G5	Q16	H3	R45	G9	R132	G4	R312	C5	R342	B6	TP59	C10
G12	G5	C89	G5	Q17	C4	R46	G9	R133	G4	R313	C5	R343	B6	TP60	C10
G13	G5	C210	F2	Q18	F2	R47	H9	R134	F3	R314	C5	R344	B6	TP61	C10
G14	K7	C211	F5	Q19	F3	R48	H9	R135	F4	R315	C5	R345	B6	TP62	C10
C36	J6	C213	F7	Q20	C4	R49	G9	R136	F4	R316	C6	R346	B6	TP63	C10
C37	K4	C214	F7	Q21	F6	R50	H10	R137	F4	R317	C6	R347	B6	TP64	C10
C38	K4	C215	G7	Q22	F6	R51	H10	R138	G4	R318	C6	R348	B6	TP65	C10
C39	K3	C216	G7	Q23	F7	R52	H10	R139	G4	R319	C6	R349	B6	TP66	C10
C40	K4	C217	G3	Q24	F8	R53	H10	R140	G3	R320	C6	R350	B6	TP67	C10
C41	L7	C217	F7	Q25	C8	R54	G10	R141	F6	R321	C6	R351	B6	TP68	C10
C42	L6	C218	F7	Q26	C7	R55	G10	R142	F5	R322	C6	R352	B6	TP69	C10
C43	J8	C219	K3	Q27	K3	R56	G10	R143	F5	R323	C6	R353	B6	TP70	C10
C44	K7	C220	M5	Q28	L5	R57	G10	R144	G5	R324	C6	R354	B6	TP71	C10
C45	K7	C221	M5	Q29	M3	R58	G10	R145	G5	R325	C6	R355	B6	TP72	C10
C46	K8	C222	M5	Q31	M6	R59	G11	R146	G5	R326	C6	R356	B6	TP73	C10
C47	K8	C223	M5	Q32	B5	R60	H11	R147	G5	R327	C6	R357	B6	TP74	C10
C48	K7	C224	L6	Q33	M8	R61	G11	R148	G5	R328	C6	R358	B6	TP75	C10
C73	G6	C225	L6	Q34	M7	R62	G11	R149	G5	R329	C6	R359	B6	TP76	C10
C74	C6	C301	K4	Q41	M3	R63	G11	R150	G5	R330	C6	R360	B6	TP77	C10
C75	J5	C302	E3	Q44	G5	R64	G11	R151	G5	R331	C6	R361	B6	TP78	C10
C77	J3	C303	L5	Q49	M5	R65	G11	R152	G5	R332	C6	R362	B6	TP79	C10
C78	F6	C304	E5	Q50	J5	R66	F6	R153	F8	R333	C6	R363	B6	TP80	C10
C79	H6	C305	E3	Q51	K4	R67	F5	R154	G5	R334	C6	R364	B6	TP81	C10
C80	C4	C307	E5	Q52	J3	R68	F5	R155	F7	R335	C6	R365	B6	TP82	C10
C81	B7	C308	M4	Q53	M3	R69	F5	R156	F8	R336	C6	R366	B6	TP83	C10
C82	B6	C309	E5	Q54	L2	R70	F5	R157	F8	R337	C6	R367	B6	TP84	C10
C83	B6	C310	K4	Q55	L4	R71	F5	R158	G7	R338	C6	R368	B6	TP85	C10
C84	B6	C311	M4	Q57	M4	R72	F7	R159	G7	R339	C6	R369	B6	TP86	C10
C85	D4	C313	J4	Q58	M2	R73	F7	R160	G7	R340	C6	R370	B6	TP87	C10
C86	E3	C315	K4	Q59	J3	R74	F6	R161	G10	R341	C6	R371	B6	TP88	C10
C87	E4	C316	K3	Q60	K3	R75	F6	R162	G10	R342	C6	R372	B6	TP89	C10

Figure 7-2. Main Board (A1) Component Locations


A1
Ø LOCK FILTER
FREQUENCY CONTROL
VOLTAGE TO C
WAVEFORM SWITCH S2
MULTIPLIER SWITCH S1
MAIN FREQ CONTROL
SHEET 1 REF
SHEET 2 C
SHEET 3 D
MULTIPLIER
1 MHZ
0.001 HZ

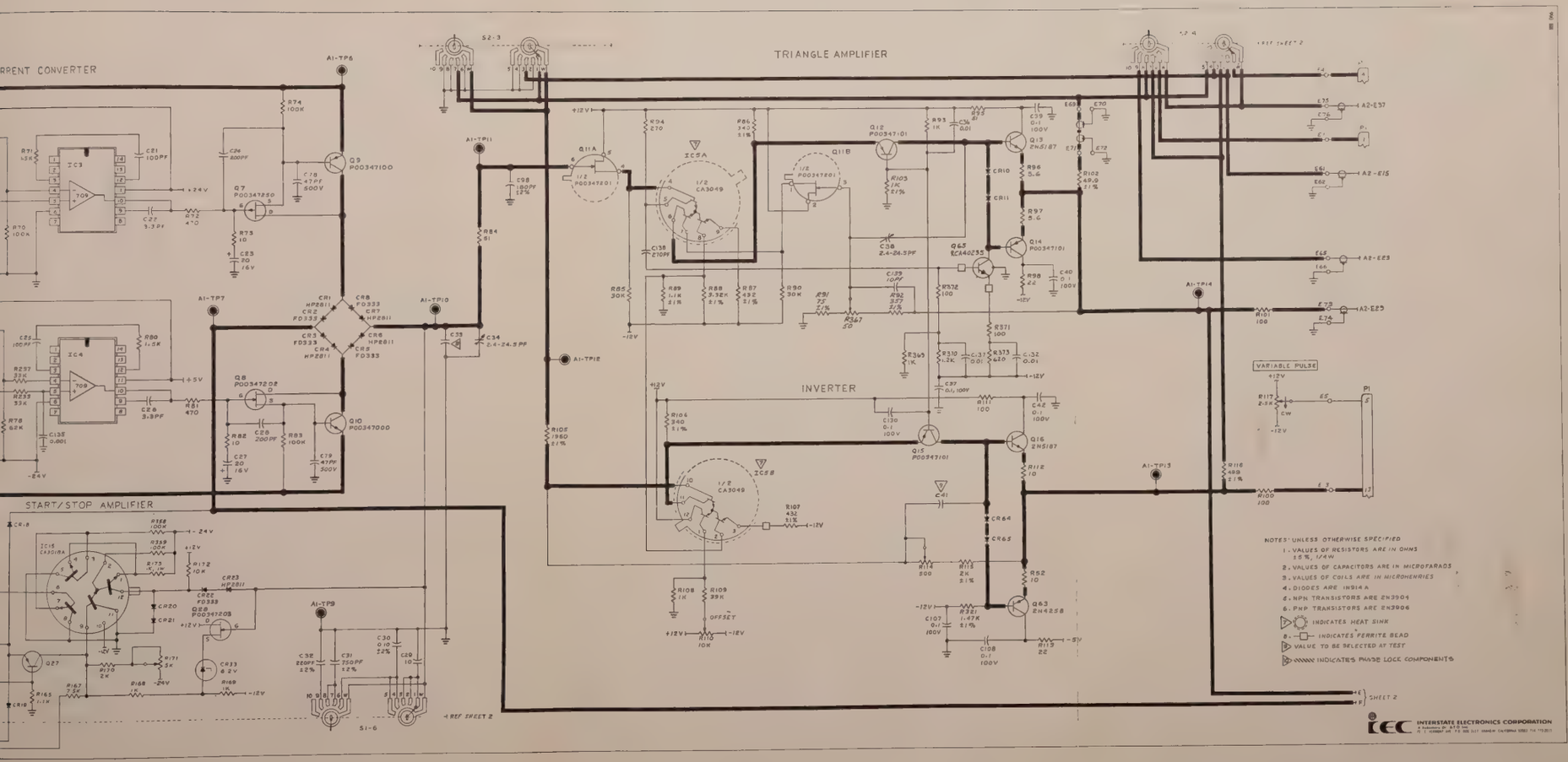
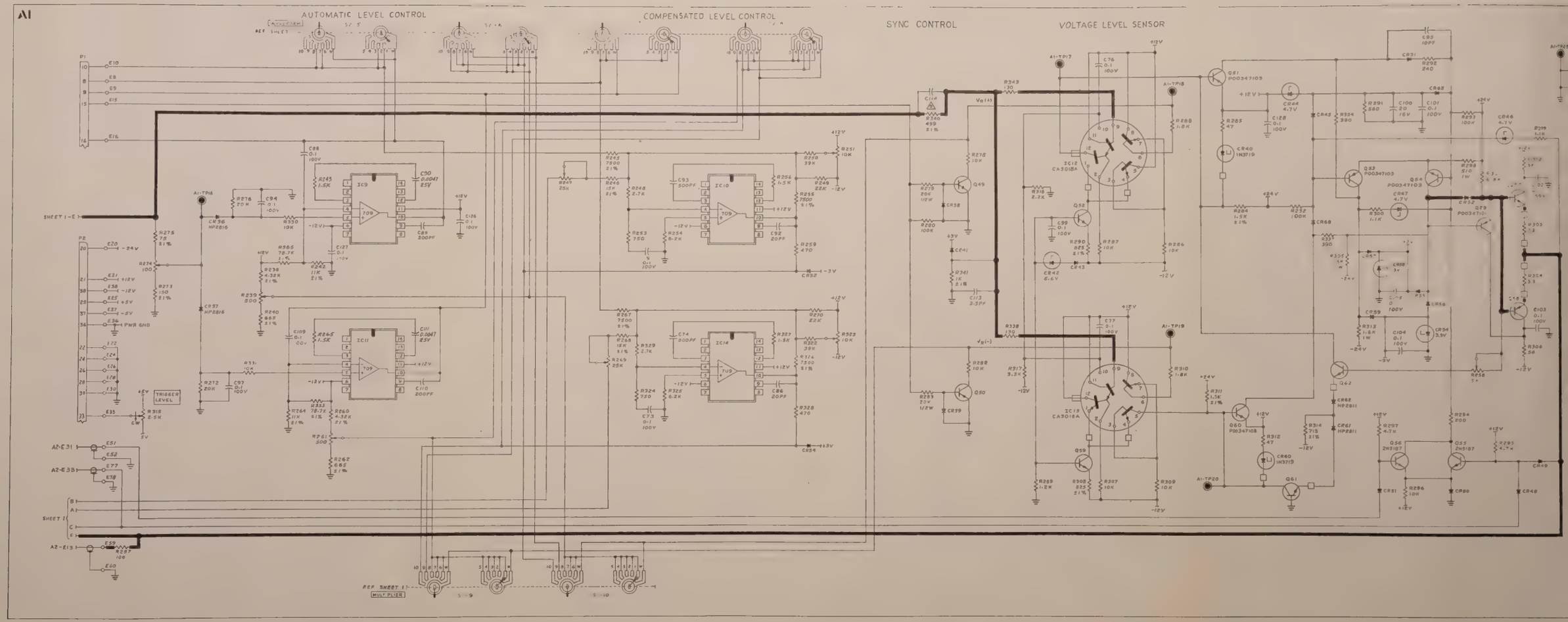

TRIANGLE AMPLIFIER
INVERTER
START/STOP AMPLIFIER
VARIABLE PULSE
OFFSET
NOTES: UNLESS OTHERWISE SPECIFIED
1. VALUES OF RESISTORS ARE IN OHMS ±5%, 1/4W
2. VALUES OF CAPACITORS ARE IN MICROFARADS
3. VALUES OF COILS ARE IN MICROHENRIES
4. DIODES ARE 1N914
5. NPN TRANSISTORS ARE 2N3904
6. PNP TRANSISTORS ARE 2N3906
INDICATES HEAT SINK
INDICATES FERRITE BEAD
VALUE TO BE SELECTED AT TEST
INDICATES PHASE LOCK COMPONENTS
INTERSTATE ELECTRONICS CORPORATION

Figure 7-3. Main Board (A1) Schematic (Sheet 1 of 2 sheets)


A1
AUTOMATIC LEVEL CONTROL
COMPENSATED LEVEL CONTROL
SYNC CONTROL
VOLTAGE LEVEL SENSOR
REF SHEET
SHEET 1-E
SHEET 1
A2-E31
A2-E33
A2-E13
TRIGGER LEVEL
PWR GND
REF SHEET 1
MULT PLIER
S-9
S-10
IC9
IC10
IC11
IC14
IC12 CA3018A
IC13 CA3018A
709
A1-TP16
A1-TP17
A1-TP18
A1-TP19
A1-TP20
+12V
-12V
+24V
-24V
+5V
-5V
+3V
-3V

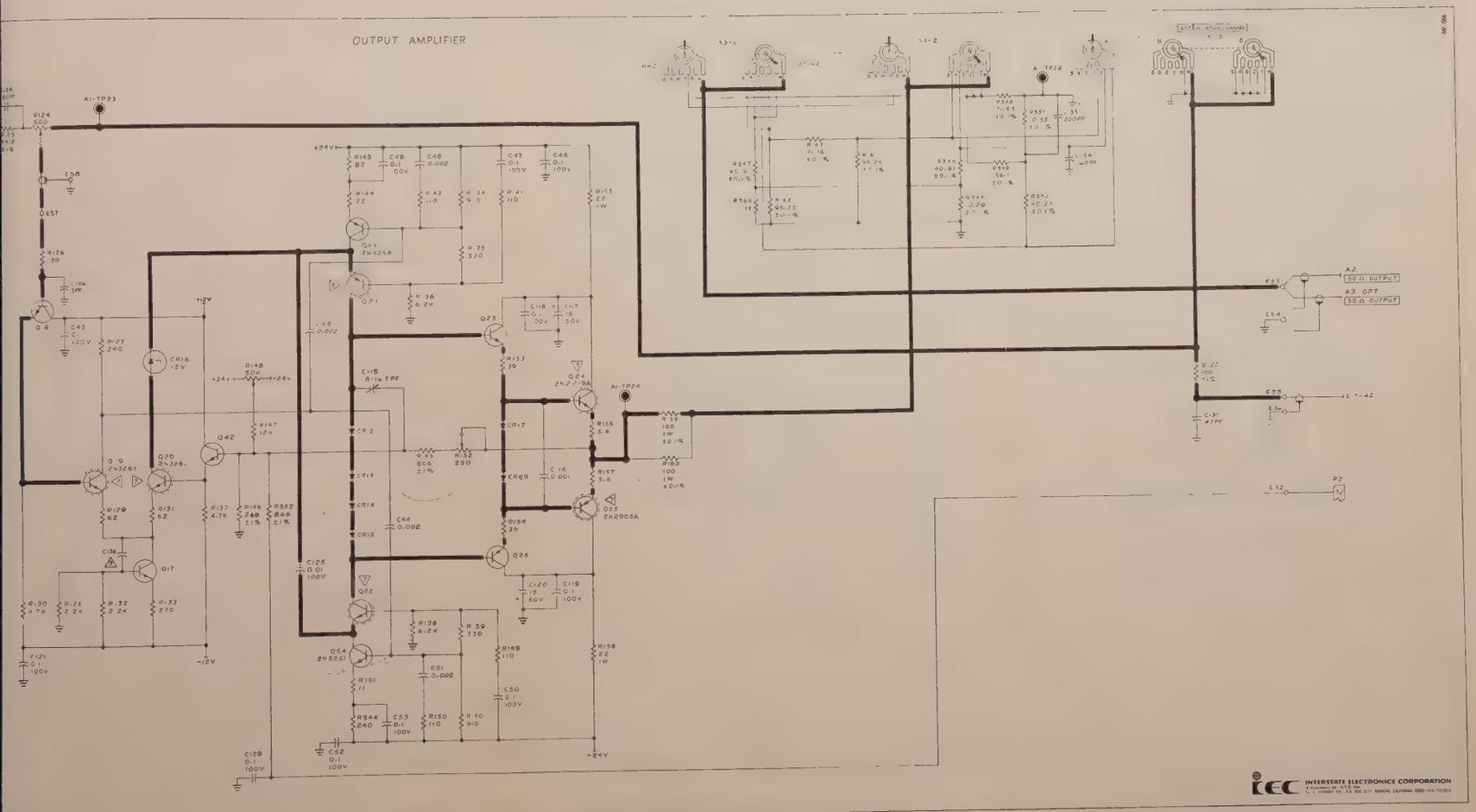


Figure 7-3. Main Board (A1) Schematic (Sheet 2 of 2 sheets)

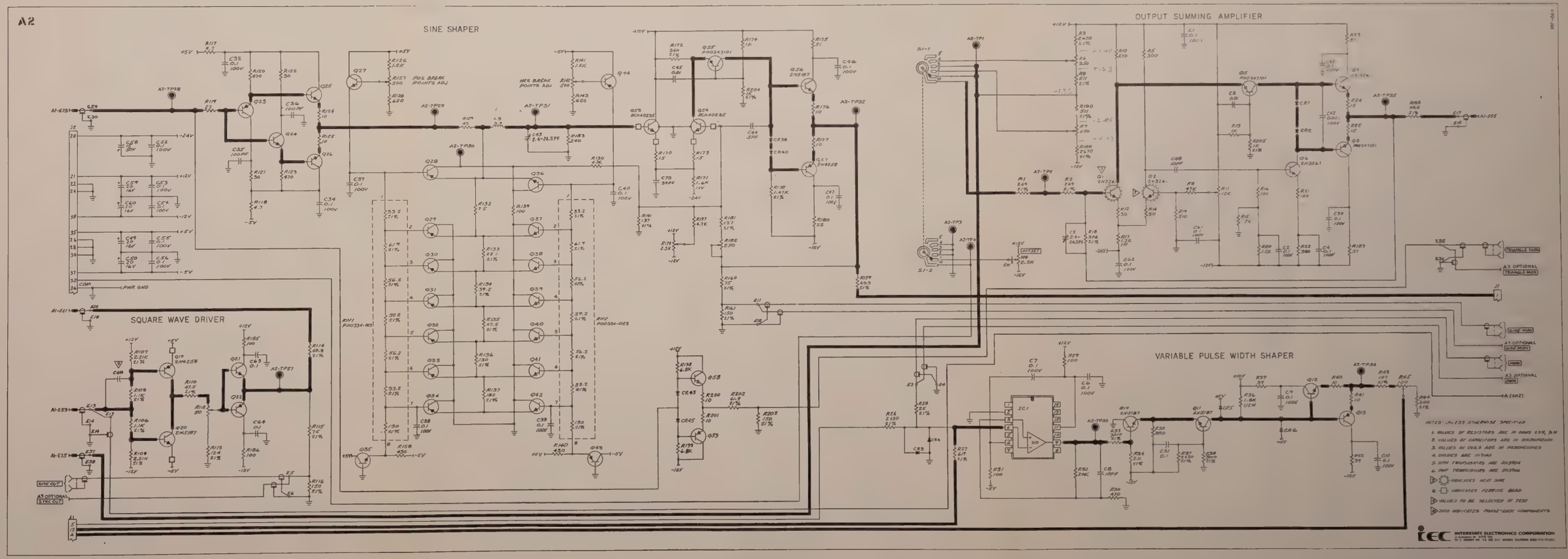


Figure 7-5. Auxiliary Board (A-2) Schematic (Sheet 1 of 2 sheets)

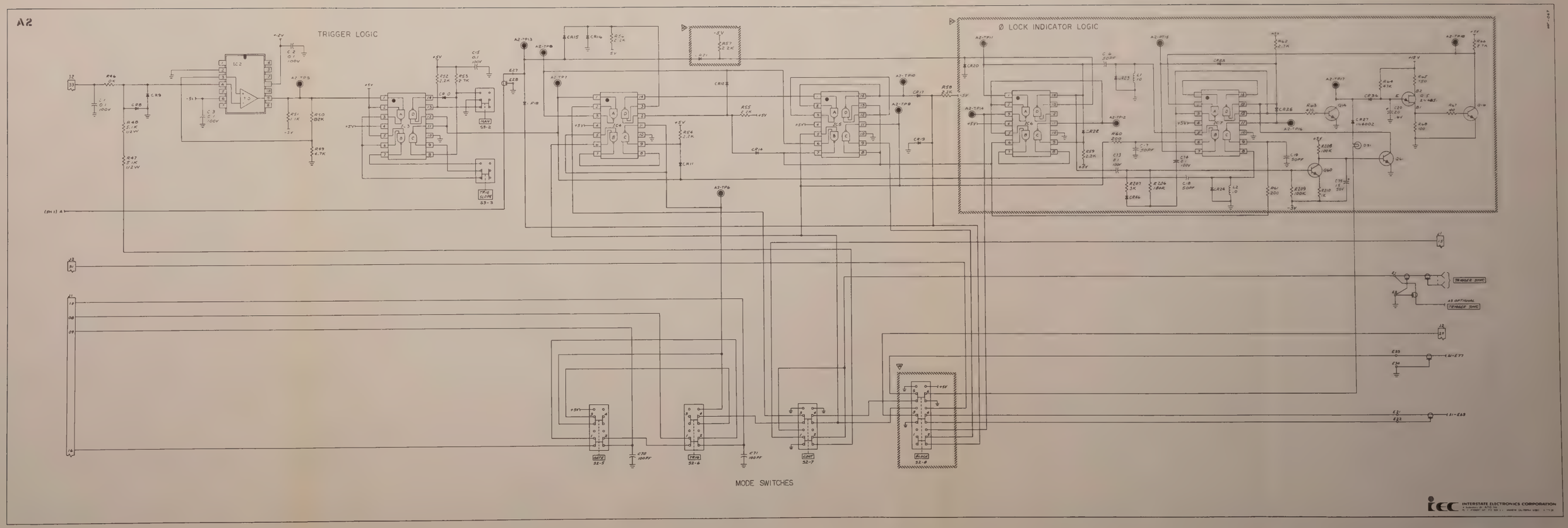
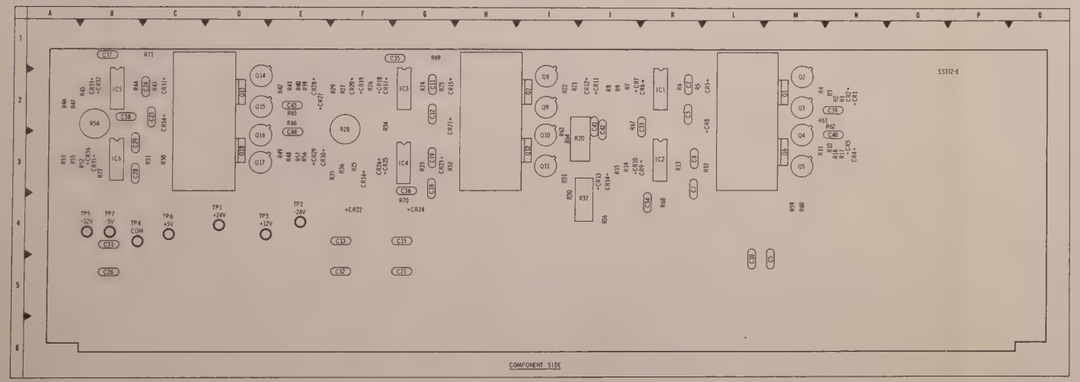


Figure 7-5. Auxiliary Board (A2) Schematic (Sheet 2 of 2 sheets)



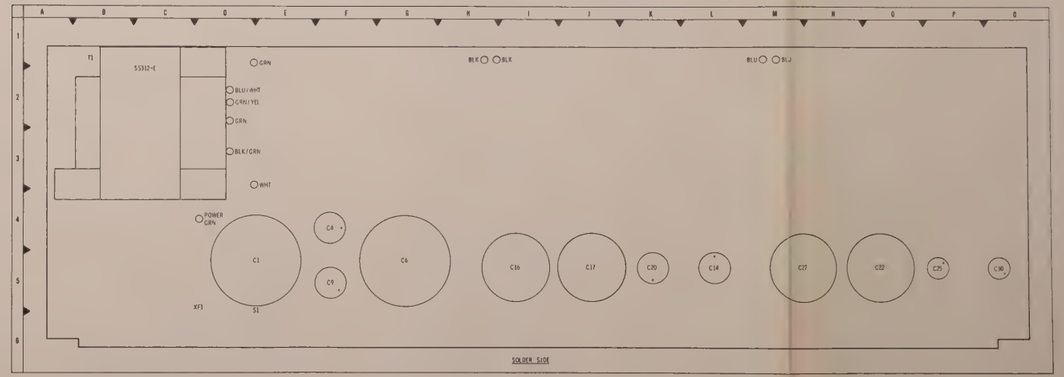


TABLE 7-3 POWER SUPPLY BOARD A3 COMPONENT LOCATIONS

REF DESIG	ZONE	REF DESIG	ZONE	REF DESIG	ZONE	REF DESIG	ZONE
FAINT							

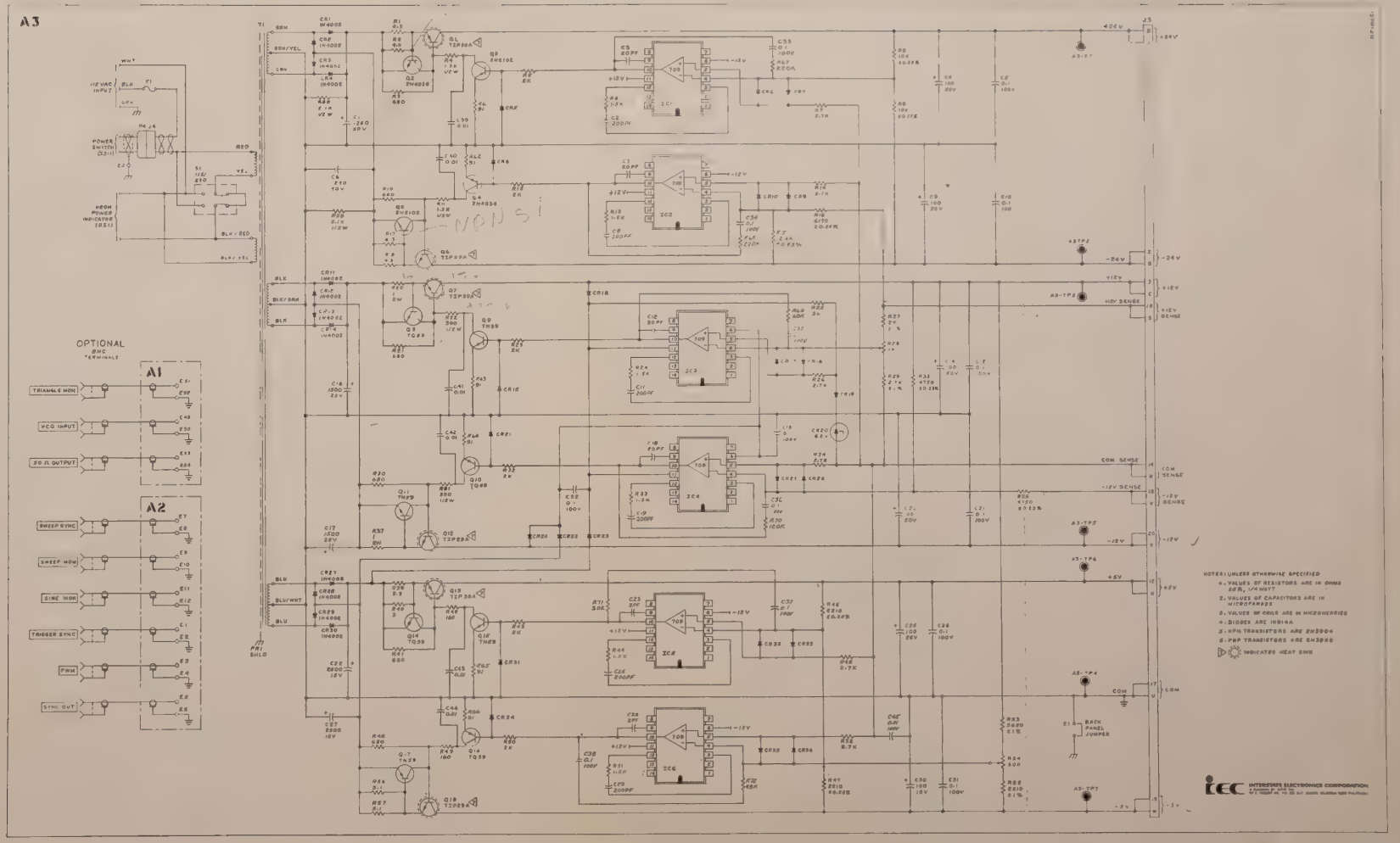


Figure 7-7. Power Supply Board (A3) Schematic

COMPONENT SIDE
S5312-E
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
IC1
IC2
C1
C2
C3
C5
C7
C8
C10
C33
C34
C39
C41
C42
C46
R1
R2
R3
R4
R5
R6
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16
R17
R18
R20
R21
R22
R30
R31
R37
R43
R44
R59
R60
R61
R62
CR1+
CR2+
CR3+
CR4+
CR5+
CR6+
CR7+
CR8+
CR9+
CR10+
CR11+
CR12+
CR13+
CR14+
T1
S5312-E

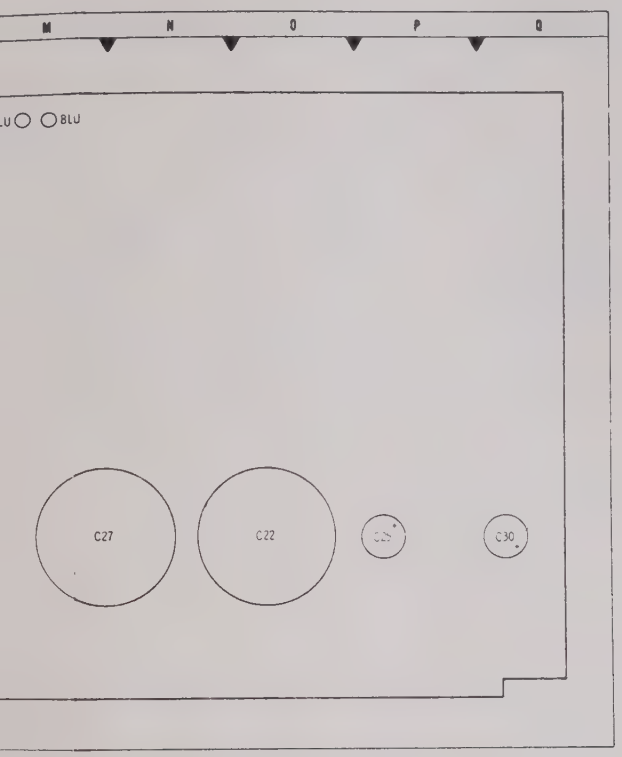


TABLE 7-3. POWER SUPPLY BOARD (A3) COMPONENT LOCATIONS

MF-1044A

REF DESIG	ZONE	REF DESIG	ZONE	REF DESIG	ZONE	REF DESIG	ZONE
FRONT		CR14	J3	R1	N2	R49	E3
C2	K2	CR15	G2	R2	N2	R50	D3
C3	K2	CR16	F3	R3	N2	R51	C3
C5	M4	CR17	F2	R4	M2	R52	B3
C7	K3	CR18	F4	R5	K2	R53	A3
C8	K3	CR19	F2	R6	F2	R54	B2
C10	L4	CR20	F1	R7	L2	R55	A1
C11	G2	CR21	G2	R8	J2	R57	E3
C12	G2	CR23	G3	R9	J2	R59	M4
C13	F4	CR24	G4	R10	N3	R60	M4
C15	G4	CR25	F4	R11	M2	R61	N2
C18	G3	CR26	F3	R12	L2	R62	N2
C19	G3	CR27	E2	R13	K3	R63	I2
C21	G5	CR28	E2	R14	J3	R64	I2
C23	C2	CR29	E3	R15	J3	R65	F2
C24	C2	CR30	E3	R16	J4	R66	E2
C26	B5	CR31	C2	R17	N3	R67	J2
C28	B3	CR32	B2	R18	N3	R68	K4
C29	B3	CR33	B2	R20	J3	R69	G1
C31	B4	CR34	C2	R21	I2	R70	G4
C32	F5	CR35	B3	R22	I2	R71	D1
C33	K2	CR36	B3	R23	G2	R72	B3
C34	K4	CR37	K2	R24	G2	TP1	D4
C35	G1	CR38	K3	R25	F3	TP2	E4
C36	G3	CR39	G2	R26	F2	TP3	E4
C37	B1	CR40	G3	R27	F2	TP4	B4
C38	B2	CR5	B2	R28	F2	TP5	B4
C39	N2	CR6	B3	R29	F2	TP6	C4
C40	N2	CR7	M2	R30	J3	TP7	B4
C41	J2	CR8	M2	R31	I2	REAR	
C42	J2	CR9	M2	R32	G3	C1	E5
C43	E2	CR10	M3	R33	G3	C4	F4
C44	E3	CR11	M3	R34	F2	C6	G5
CR1	N2	CR12	M3	R35	F3	C9	F5
CR2	N2	CR13	I2	R36	F3	C14	G5
CR3	N3	CR14	I2	R37	J3	C16	I5
CR4	N3	CR9	I2	R39	E2	C17	I5
CR5	L2	CR10	I3	R40	E2	C20	K5
CR6	K2	CR11	I3	R41	E2	C22	G3
CR7	J2	CR12	I3	R42	E2	C25	F5
CR8	L2	CR13	D2	R43	C2	C27	N5
CR9	K3	CR14	D2	R44	B2	C30	G5
CR10	J3	CR15	D2	R45	B2	S1	E5
CR11	J2	CR16	D3	R46	A2	T1	C5
CR12	J2	CR17	D3	R47	A2		
CR13	J3	CR18	D3	R48	E3		

Figure 7-6. Power Supply Board (A3) Component Locations

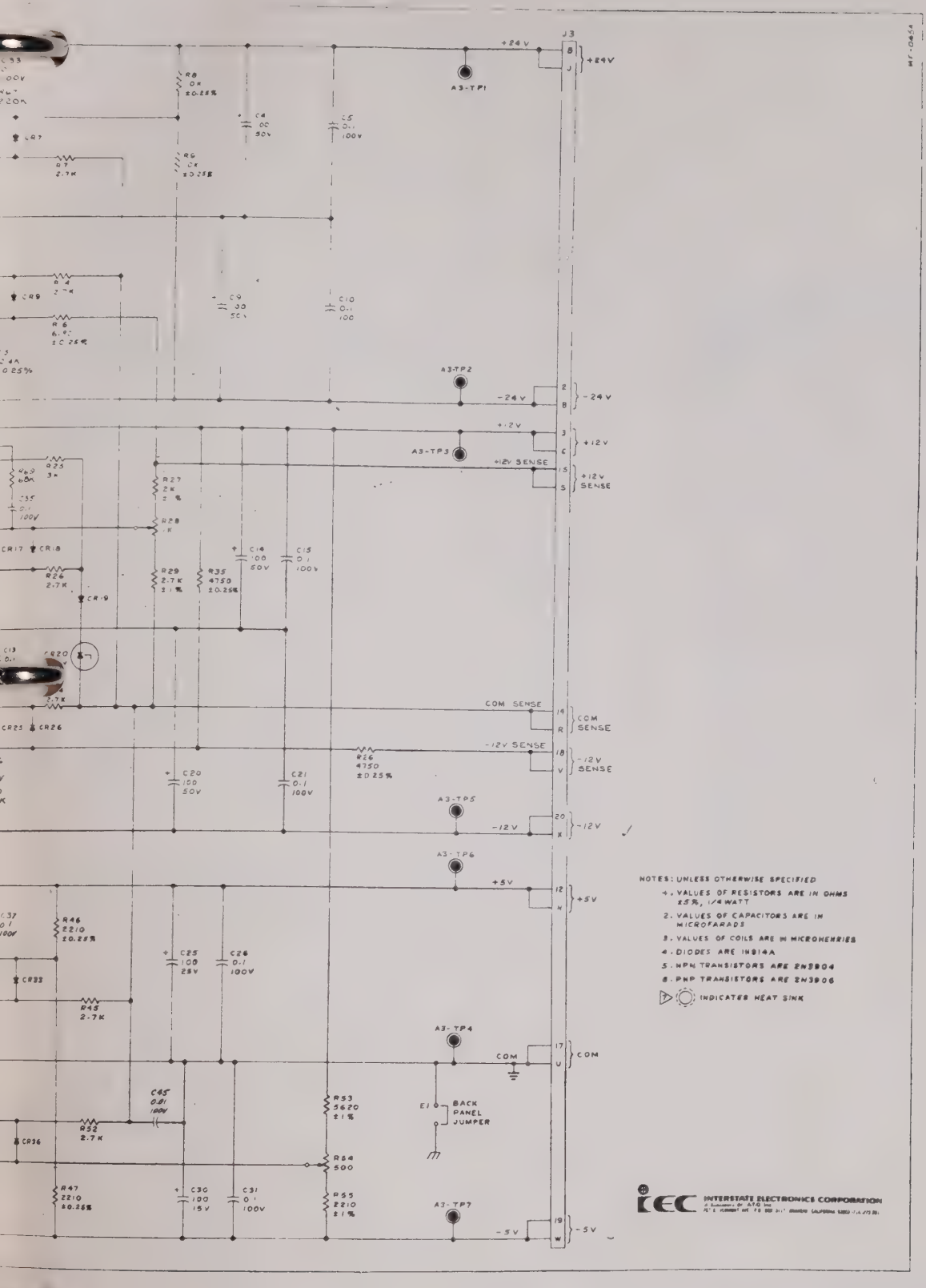
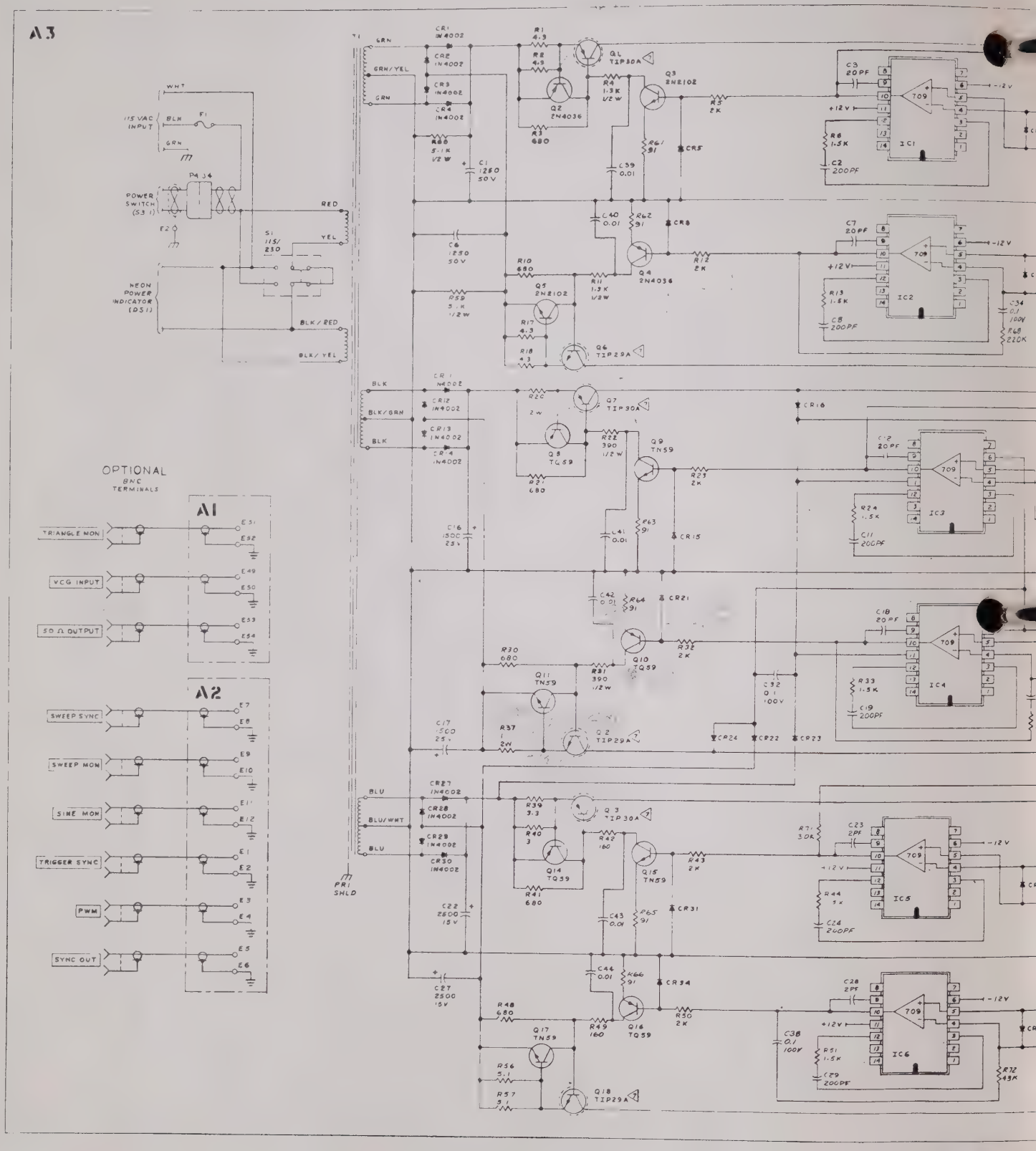
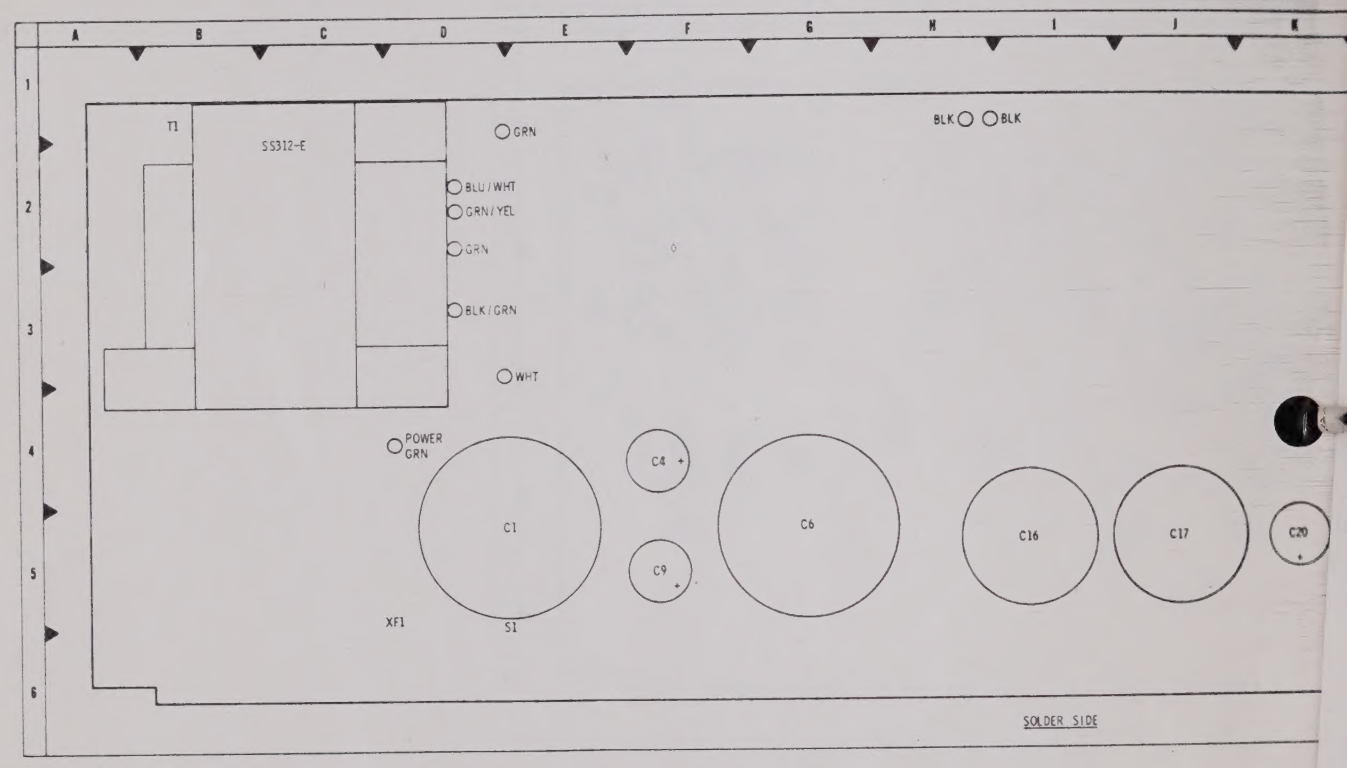
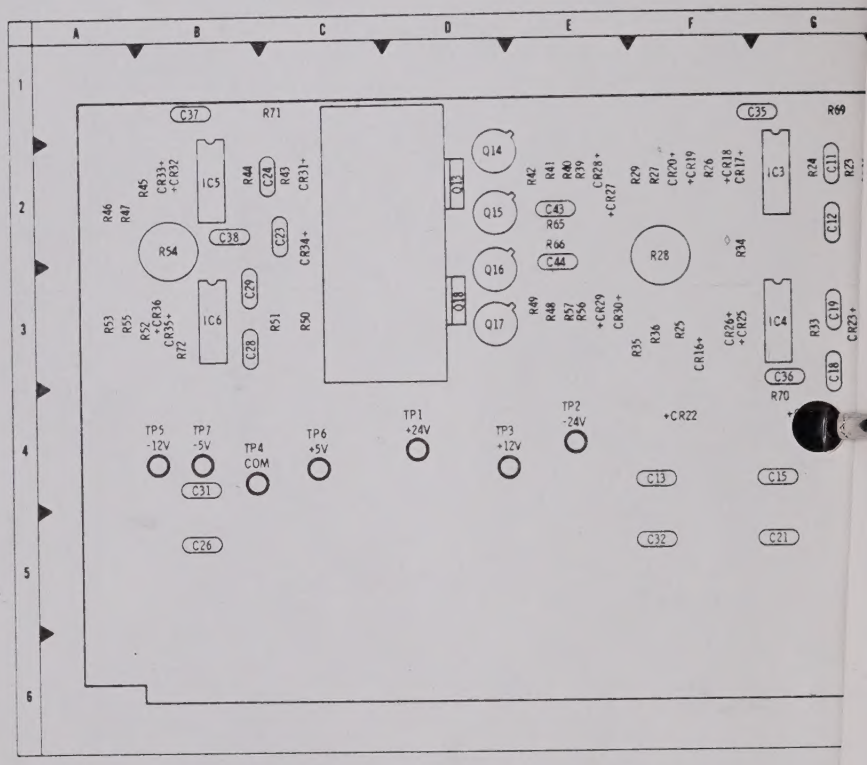


Figure 7-7. Power Supply Board (A3) Schematic


A3
A1
A2
OPTIONAL
BNC
TERMINALS
TRIANGLE MON
VCG INPUT
50 Ω OUTPUT
SWEEP SYNC
SWEEP MON
SINE MON
TRIGGER SYNC
PWM
SYNC OUT
115 VAC INPUT
POWER SWITCH (S3 1)
NEON POWER INDICATOR (DS1)
S1 115/230
F1
F2
P4 J4
T1
PRI SHLD
IC1
IC2
IC3
IC4
IC5
IC6
709
+12V
-12V


A
B
C
D
E
F
G
H
I
J
K
1
2
3
4
5
6
T1
SS312-E
GRN
BLU/WHT
GRN/YEL
GRN
BLK/GRN
WHT
BLK
BLK
POWER
GRN
C1
C4
C9
C6
C16
C17
C20
XF1
S1
SOLDER SIDE


A
B
C
D
E
F
G
1
2
3
4
5
6
C37
R71
C35
R69
IC5
IC3
IC6
IC4
R54
R28
C43
C44
C38
C31
C26
C13
C15
C32
C21
C36
R70
Q14
Q15
Q16
Q17
Q12
Q18
TP5 -12V
TP7 -5V
TP4 COM
TP6 +5V
TP1 +24V
TP3 +12V
TP2 -24V
+CR22